DESIGN AND FABRICATION
OF AN ANALOG VOLTAGE TO DUTY CYCLE GENERATOR

Final Report

February 1969

Contract No. NAS7-100

Task Order Number RD-28

JPL Contract Number 951306

Prepared for

California Institute of Technology
Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, California

by

Westinghouse Research Laboratories
PITTSBURGH, PENNSYLVANIA 15235

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SUMMARY

This report covers work on a voltage to duty-cycle converter fabricated on four silicon integrated circuit chips assembled in a single package. It will perform the essential signal processing functions of a precision power regulator system using duty-cycle control of the power output stages. The converter subsystem requires large value stable capacitors and high precision stable resistances which are obtained by using a hybrid tantalum film-planar silicon integrated circuit technology. In this technology, the capacitors have tantalum oxide (TaO_5) for the dielectric and the precision resistors are made of tantalum nitride (TaN).

The four circuits in the subsystem are a precision voltage reference supply, a gain-stable error voltage amplifier, a stable triangle waveform generator, and a comparator with output logic. Stability and linearity are achieved over an operating temperature range of -10°C to +75°C, not only through the use of the stable tantalum film components in sensitive areas, but also by the use of resistance ratios to determine well-defined voltage levels. Also, use is made of adjoining transistor pairs for input stages of difference or comparison amplifiers where minimum drift is needed. The electrical performance of the convertor is the conversion of a 10.000 volt $\pm$ 0.050 volt input signal into a power gate output duty-cycle ranging from 3% at 10.05 volt input to 97% at 9.95 volt input. The linearity is better than 2.5% at a basic repetition rate of 2.5 KC $\pm$ 10%. Equivalent input stability over the operating temperature range is 0.025 volts or better, or better than 0.25% of the 10 volt input.

The work performed was carried out initially by the Westinghouse Molecular Electronics Division, West Coast Department, and was completed by the Information Devices Department of the Westinghouse Research Laboratories. The work at the Research Labs was carried out by P. R. Malmberg, M. J. Geisler, P. Gutknecht, W. D. Frobenius, M. M. Sopira and P. D. Blais, with the assistance of the staff of the Fabrication Facility of the Information Devices Department, which is hereby gratefully acknowledged.

1. INTRODUCTION

The requirement for this project was the design and fabrication of an Analog Voltage to Duty Cycle Generator. The system converts a variable low power level DC signal into a digital output. The system will be used for a precision power supply. An integrated version of the Analog Voltage to Duty Cycle Generator offers increased reliability over the present discrete component version. From considerations of reliability it was desirable to make the system with as few semiconductor chips as possible and to enclose it in a single package.

The system requires four major elements: a precision reference voltage source, a comparator amplifier, a duty-cycle reference generator and an output driver. Several alternative methods are available for achieving the required function, but from considerations of suitability for integration the choices narrow to either an analog or digital ramp generator. Both of these alternatives were tried in breadboard form, and it was ultimately decided the analog triangle function generator would best serve the required purpose, although this did require large capacitor values to achieve the required time constants. The use of tantalum oxide capacitors and tantalum or tantalum nitride thin film resistors on the silicon oxide surface of the chips, a hybrid approach, allows the high value capacitors and precision resistors to be made without undue sacrifice of area. Precise values of resistor ratios are required to establish accurately the reference voltage level, to determine the gain of the reference amplifier, and to establish the time constants for the triangle function generator. Consideration of power dissipation and temperature stability must also be made in determining the division of the system into separate chips and the method of final encapsulation since the operating temperature of the chips is a major factor in determining the ultimate reliability of the system.

2. TECHNICAL DISCUSSION

2.1 System Design Considerations

The Jet Propulsion Laboratories Advanced Development Engineering Note No. 342-50 gives a concise description of the overall systems requirement and reads as follows:

1.0 General Requirements*

1.1 In all duty cycle type of regulators there is a circuit that converts a variable, low power level, D.C. signal, to a digital output. The digital output may have several forms, but in all forms the one-level time, or "on" time, portion of the cycle is proportional to the D.C. input signal. The present, "least hardware" approach to this function is to drive saturable reactors with a square wave, and drive the control winding in proportion to the D.C. signal level. The use of reactors in this way reduces the total number of components and so is preferable to an all transistor approach. This reduction in component parts does not necessarily increase reliability in the microcircuitry approach. It will be a requirement to generate a reliable, least hardware logic for such a circuit and to "build" it on as few chips as

*Jet Propulsion Laboratories Engineering Note No. 342-50 possible (one to two being most desirable). There are two general types of such regulators and they re-require different signals. It is best if we can use the same circuit for both types by a simple manipulation of its outputs externally.

1.2 In one type, the down regulator, the required signal is single ended in nature. That is, it turns on one switch (several transistors may be in parallel, but it is one switch) for the on part of the cycle, and turns it off for the off part of the cycle. (See Figure 1 for a graphical explanation). The other type, a booster regulator, requires what may be called a double-ended signal. That is, one part of the signal drives one switch on for a variable part of half of the total cycle time and the other part of the signal drives another switch on for a variable part of the remaining half of the cycle time (see Figure 2). The power amplifier indicated in the diagram means that the functional block referred to need only supply "signal" power. The parts of the signal are separated by virtue of the way they are applied to the switch. The "on" signal for B, though applied to A, can only act on A to drive it harder off.

1.3 For flexibility, the signals can be transformer coupled to the switches with D.C. restoration at the switch. The wave form in Figure 1 can be synthesized from that in Figure 2 by the use of a transformer and diodes. This leads to the possibility of obtaining either from two proper sources. If the output of the functional block were really two outputs as shown in Figure 3, then either type of signal could be derived by proper external manipulation.

2.0 Specific Requirements*

2.1 Electrical

2.1.1 Repetition rate for either output - 2.5 KC ± 10%

2.1.2 Output level

"1" level - Output will be high impedance to return with maximum leakage of 5 microamps at 20 volts and 75°C (turned off transistor collector)

"0" level - Output to return 0.5 volts maximum at -50 milliamps maximum output current over line and temperature variation (a saturated transistor)

2.1.3 Deleted

2.1.4 Deleted

2.1.5 Input power - 20V D.C. ± 1V (this implies internal regulation)

*As Amended by Technical Direction Memorandum 12/9/65

2.1.6 Input signal

Input signal center value plus 10 volts $\pm$ 0.01 volts

Input signal source impedance 10 K ohms $\pm$ 5%

2.1.7 Circuit Sensitivity: - Nominally + 1% in output duty cycle change for -1 millivolt signal input change at + 20°C input signal center value, plus 0.05 volts will yield an output duty cycle less than 3% and input signal center value -0.05 volts will yield an output duty cycle greater than 97%.

2.1.8 Output linearity - If the transfer of output duty cycle (ordinate) versus input signal (abscissa) is drawn, ideally it should be a straight line. We shall define a linearity tolerance to be a vertical displacement of the true value from a straight line drawn through the 97% and 3% true values. The maximum vertical departure at any input signal from the straight line shall be $\pm$ 2.5 duty cycle percentage points. (Use the ordinate scale to determine the departure.)

2.1.9 Output time symmetry - During steady state conditions (any constant value input signal), the "on" time of the signal from one output line shall be within .5% of the "on" time of the other output line. In addition, the half period time (Figure 3) which determines the start of output number 2 shall be within ± .25% of the absolute value of half period time.

2.1.10 Temperature - 10°C to + 75°C

2.1.11 Rise and fall time - .5 microseconds maximum from zero to specified output and vice versa.

2.1.12 Circuit Stability (with both input power variations and temperature variations). The signal input required per any given duty cycle must not vary by more than ± 0.025 volts.

2.2 Mechanical

Any suitable hermetically sealed container with leads arranged to permit mounting on a circuit board and to be welded to connecting leads on the opposite side of the board.*

*End of Jet Propulsion Laboratory Engineering Note No. 342-50.

2.2 Discussion of Possible Approaches

A number of technical approaches can be used to fulfill the requirements of this system; therefore, the first requirement is to investigate each method and then to evaluate which is the most suitable for integrated circuit fabrication. The following systems have been considered:

1. DC-controlled Asymmetrical Multivibrator.
2. Clocked Multivibrator.
3. Analog Ramp Generator.
4. Digital Ramp Generator.

Each of these approaches will now be discussed for the purpose of establishing the most optimum system.

2.2.1 DC-Controlled Asymmetrical Multivibrator

The variable Duty Cycle Multivibrator approach is probably the most common control system in a series switching regulator. This approach is shown in Figure 4. This system is described in detail on page 463 of "Transistor Circuit Design," McGraw-Hill Book Company, Inc. It has the advantage of simplicity from a "number of components" standpoint; however, there is one major incompatibility between this approach and the system specification, namely this system has a widely varying repetition rate. For the requirement of from 3 to 97% in duty-cycle, the repetition rate will vary by a factor of 10. This factor alone has disqualified this otherwise attractive approach.

2.2.2 Clocked Multivibrator

This system is a modification to approach "1" but would maintain a stable repetition rate. The block diagram of this system is shown in Figure 5. A clock circuit would be used to develop a 2.5 KC repetition rate. This would be used to reset the multivibrator to the "on" condition. A buffer would be placed between the clock and multivibrator to insure that the clock frequency is not effected by the input voltage.

The multivibrator would be monostable, and the "on" time would be determined by the DC level of the amplifier. This would be accomplished by using the amplifier output as the reference voltage to change the duration determining time-constant of the multivibrator.

This approach appears feasible, but presents two major problems. The first is that the resistors and capacitors associated with repetition rates of 2.5 KC are necessarily large. For instance, a simple RC circuit with time constant equal to 400 micro-seconds could consist of a 500 pf capacitor and an 800 K ohm resistor. Obtaining either of these values would be bordering on "the State of the Art." Undoubtedly, thin film techniques would be required.

The second obstacle is that a very complex control multivibrator would have to be developed. In fact it might prove impossible to develop such a circuit when one adds the restrictions of using integrated components.

2.2.3 Analog Ramp Generator

In essence this system would compare the power supply output reference voltage with a linearity decreasing voltage to determine the duty cycle waveforms shown in Figure 7. These waveforms illustrate the relationship between the ramp voltage and the duty cycle.

The clock would operate at a nominal 2.5 KC. The clock output would reset the ramp generator. The ramp generator produces a linear change in voltage with respect to time. This is one input to the comparator amplifier. The other input is the voltage established using the input signal (20 $\pm$ 0.1 VDC) and the reference element. The comparator amplifier will then control the switch duty cycle determined by the relative magnitudes of it's two inputs.

The realization of the time constant for the clock will have the same problems as the clock in Approach "2".

Figure 8 illustrates the ramp generator-control circuit.

The clock circuit triggers a monostable multivibrator whose pulse width is 3% of the duty cycle. This one-shot shorts out C_1 by turning Q_1 on in the inverted mode. At the same time the one-shot holds Q_2 off through a saturated transistor. When the multivibrator changes states, Q_2 turns on and performs the function of a constant current generator. At the same time C_1 is no longer shorted. At the moment of Q_1 turning off, the voltage on both sides of C_1 is determined by the voltage divider R_2 and R_3 across reference Z_1. As time elapses a constant current will be supplied to C_1 changing its voltage linearly in a negative direction.

The output of the ramp generator and the "input signal" from voltage divider R_7 and R_8 are then fed to the comparator amplifier. At the time the one-shot shorts out C_1 the ramp generator output exceeds the "input signal," so the comparator will switch "on." The amplifier will remain "on" until the ramp generator decreases to a value below the "input signal" at which time it turns off. The amplifier will remain in this state until the "one-shot" is retriggered.

This approach is very susceptible to parameter drift with both temperature and time. Component parameters for the capacitor shorting circuit and the constant current generator are also very critical.

2.2.4 Digital Ramp Generator

A digital system approach was explored as it lends itself to integrated circuit fabrication. This investigation produced the block diagram in Figure 9. A more complete block diagram is shown in Figure 10. This approach is identical to the preceding system except that a digital ramp generator replaces the analog ramp generator. The first significant feature is that the clock frequency is now 320 KC rather than 2.5 KC. This means that the basic components which control the time constant, can be reduced by a factor of 128. This makes them readily producible in an integrated circuit. In addition, the mechanism for generating the ramp voltage in this system is not sensitive to parameter drifts.

Of these four approaches, the first was rejected because of the varying repetition rate, and the second because of requiring components at the limit of the existing art. The third and fourth approaches are similar, the major difference being in the method of generating the linear ramp. Because of the large RC product required by the third approach in the analog ramp generator, it was originally felt that the fourth approach, using a binary counter and D/A converter to furnish a staircase ramp with 128 discrete levels would offer the best method of realizing the desired subsystem performance. Accordingly, initial engineering and design effort was expended on this digital implementation of the converter, with the knowledge that the analog ramp generation would be an alternative to fall back on if difficulties should arise in the digital method.

2.3 Circuit Design Considerations

2.3.1 Digital System Development

2.3.1.1 System Description

The logic diagram of the selected system (the digital ramp generator) is shown in Figure 10.

The basic approach is to develop a ramp voltage which can be compared with the incoming signal. At the time of coincidence, the output will change from a "1" to a "0" state, thus controlling the duty-cycle of a series switch in a switching-mode power supply regulator.

The logic control of this system is straightforward. A 320 KC clock drives an eight bit counter. The first seven bits provide the control to the "Ramp Generator". This portion of the counter also provides the repetition rate, which is 320 KC $\div$ 128 = 2.5 KC.

The eighth flip-flop controls the two outputs so that they are "on" during alternate periods. This is accomplished by the use of the two output gate drivers. This logic design, which utilizes a single clock, insures that the device will meet the output-time-symmetry requirements.

Ramp Generator -- The ramp generator circuit is shown in simplified form in Figure 11.

This circuit is a standard analog to digital converter. The only unique feature is that the reference input is set at +10 volts by the resistor divider network. This is necessary since there is no negative supply potential available to use the amplifier in the normal configuration. The amplifier use in this application is as an inverting amplifier.

The output will go as far toward ground as necessary to balance +10 volts on the inverting terminal of the amplifier. When all the switches are on and all the parallel resistors are conducting, an equivalent resistance of 1K is generated. Since the feedback resistor is 1K also, the output of the amplifier must go to zero volts to produce a +10 volts at the inverting terminal. When all the switches are off only the 256K resistor is conducting. The output of the amplifier must go to almost 10 volts to produce 10 volts at the inverting terminal.

Since the output of the amplifier must be negative with respect to the input terminals, it was necessary to bias the input terminal to a positive voltage. The resistor divider can also be used to correct any offset in the amplifier.

In the above configuration the resistors are gated "on" sequentially by the counter which is counting up. Every time the counter advances one step, the output voltage drops one increment of 128. This continues until the counter reaches all ones. When this occurs the output of the amplifier is zero volts. In the very next pulse the counter resets to all zeros and the output of the amplifier goes immediately to +10 volts. In this fashion a staircase approximation of the ramp function is generated.

An important point to note is that the absolute value of the resistors is not important in this circuit as all voltage values are derived from resistor ratios. This is significant as diffused resistors do change with temperature but they will all track proportionally.

It should also be noted that theoretically end points of 0% duty cycle and 100% duty cycle can be achieved since the system is linear in these regions.

Precision Reference Source -- Figure 12 shows the schematic of the precision reference source.

This consists primarily of a Zener diode with three forward conducting diodes and a pre-regulator. The pre-regulator is necessary to achieve a high degree of stability. The output of the reference element with 4 ma current (cross-over point) is 10.40 volts. It is therefore necessary to scale down the input voltage to the same range with resistors. This provides the reference to compare with the input voltage.

Using an amplifier with controlled gain, the error voltage is amplified to be +10 volts for the maximum voltage of 20.1 volts. See Fig. 13.

When the input voltage is 19.9 volts (20.00 - .1 volts) the output of the amplifier is zero volts. The peculiar feedback arrangement that is necessary is due to the fact that the amplifier is unipolar in output.

<u>Output Circuit</u> -- The output circuit is a combined "and" gate and power driver. A simplified schematic is shown in Figure 14.

If either input is grounded then Q_1 and Q_2 are "off". If both inputs are open (+ 20V) then the voltage at point "A" is determined by the ratio of R_1 and R_2. This resistor node has a nominal voltage of 7.1 VDC. Approximately

0.7 volts is dropped across the diode, and 1.4 volts across the Darlington pair of transistors thus providing a nominal 5.0 volt output from a low impedance.

These two outputs can be used separately to provide signals to a two-phase switching circuit, or the two outputs can be shorted to provide a continuous output on a single line. This configuration thus satisfies the requirements of providing a dual function in a single design.

Comparator Amplifier -- The comparator amplifier is a derivation of Westinghouse's standard Operational Amplifier, the WS-8199. A preliminary schematic of this is shown in Figure 15. Typical parameters of the amplifier are:

Open loop gain 86 dB

Input impedance > 300 K ohms

Output impedance < 100 ohms

Gain bandwidth product > 5 MC

Output voltage swing $\pm$ 10 V

Common mode rejection > 60 dB

DC offset voltage < 5 mV

Drift < 5 μV/°C

Power dissipation $\approx$ 350 mW.

2.3.1.2 Digital Circuit Development

As the breadboard models of the various parts of digital subsystems were made and tested, various changes and improvements were found necessary over the circuits originally proposed, as represented by Figures 10 through 15. Thus the ramp generator shown in Figures 10 and 11 using weighted resistor values was replaced by that of Figure 16, using a 2-valued resistor ladder network, thereby permitting much greater ease in matching resistor values. The differential error amplifier shown in block form in Figure 13 was realized as the feedback amplifier of Figure 20, wherein the two internal feedback loops provide a stable overall voltage gain of 40 and a DC shift from the zero-error +10.00 volt input to the zero-error output of +5.0 volts. The output circuit was changed from the power diode-transistor logic (DTL) configuration of Figure 14 to the parallel transistor NAND gate of Figure 22d. Finally, the cascaded Zener diode voltage reference source of Figure 12 gave way to the feedback voltage regulator of Figure 19.

The completed breadboard version of this digital subsystem, using discrete components, was tested in conjunction with power output stages at the JPL laboratories in January, 1966.

Although performance was essentially within expectations, several problems peculiar to this digital implementation were pointed up and prompted a further consideration of the possibilities of an analog approach. Foremost among these problems was the susceptibility of the counting circuits to false triggering from system transients, thereby producing gross errors in the staircase ramp waveform. Another problem was the severe ratio accuracy requirement of the ladder network resistors. The ramp noise occasioned in the summing amplifier output by the ripple carry of the 7-bit counter was a further drawback to this digital approach. Accordingly, a detailed comparison between digital and analog implementations of the voltage-duty cycle converter was made, and is contained in the following paragraphs.

2.3.1.3 Comparison of Analog and Digital System Accuracy

Typically, analog systems rely heavily on the characteristics of a few components and become extremely complex when carried to accuracy extremes. Digital systems inherently require a large number of components, but come into their own when high degrees of accuracy are required. The crossover point is usually determined by the system requirements or device limitations.

The overall sensitivity of the Duty Cycle Generator was determined on the basis of acceptable load regulation (± .5%) and is quite in line with practical degrees of temperature stability (± .25%) which is a device limitation. The reference element and differential amplifier input pair determine the basic temperature stability of the system. Circuit complexity and accuracy of the remaining blocks must be justified by comparison with these elements.

Matching of the ladder resistors is limited by device technology and was estimated at ±0.3%. This limitation might be improved by slightly modified fabrication approaches. However, if this were done, the accuracy of the ladder supplies would have to be improved by further complexity to match the new levels of accuracy. Ultimately, the accuracy of the digital ramp would probably exceed that of the analog triangle, but further refinement does not seem justified based on system requirements and block capabilities.

In order to maximize design flexibility, the combined effect of sensitivity and linearity were limited by Jet Propulsion Laboratory to ±3%. This tolerance is spread among several contributing factors between ±0.1% and 0.5% each. This would indicate that design complexity is in line with fundamental technology limitations.

The Analog Triangle Function Generator has been designed to meet the present linearity specification of the Digital Ramp Generator.

A summary of all comparisons made in this section are listed in Table 1. In the digital approach, sensitivity is directly related to the auxiliary power supply voltage which has an accuracy of ±0.3%. This tolerance is determined by the same considerations which determine the threshold accuracy of the Bistable Level Detector in the analog system. Linearity of the digital ramp is related to the ladder ratios ($\pm$ 3%) plus the load regulation of the auxiliary supplies ($\pm$ .4%). Linearity of the triangle generator is related to the operational amplifier as discussed earlier and is better than $\pm$ 0.5%. Without further modification it appears that the accuracy of the two approaches is quite comparable.

In this system, component count for equal accuracies favors the analog approach, as indicated in Table II. However, consideration must be given to the types and reliability of the components involved. It turns out here that all of the components except capacitors are quite comparable in reliability (including diodes versus transistors). The TEOS capacitor used in the binaries can be a prime factor in the yield and reliability of the binaries as can the tantalum capacitor in the analog system. A component count comparison of the final system with the earlier design is given in Table III.

As shown in Table IV, the digital approach requires 2 watts of power dissipation even after redesign of the binaries, while the analog approach requires 1.3 watts. 1.3 watts would allow operation in free air, but is not advisable from load regulation considerations. In both systems device dissipation will be somewhat a function of duty cycle (±10%) and would cause drift in the reference element if used in free air. A comparison of system power requirements, including that of the final design, is shown in Table V. Chatter in the duty cycle of the digital system is caused and/or magnified by the presence of high frequency spikes in the amplifier and on the ramp. These spikes may be reduced by various methods of ground, power supply isolation and shielding, but remain a problem in the digital system.

At this point of development, it was not obvious whether switching transients within the regulator itself would be adequately ignored by the Duty Cycle Generator, but this problem was the case in either the analog or digital approach. This problem could be solved by a circuit which would limit the output to one pulse per cycle. Frequency shaping of the amplifier for loop stabilization is limited by increased sensitivity to high frequency spikes.

In the digital system, a minimum of two chips are needed, considering only the process differences required for high speed digital transistors and high beta analog units. Yield measurements may increase the number.

The analog system requires a minimum of one chip, but will be more practical from the fabrication point of view, if at least two are used. Again, yield requirements may increase this number. There is very little difference in the number of jumper bonds since they would be used primarily between functional blocks when necessary.

2.3.2 Analog System Development

2.3.2.1 Analog System Description

At the time of transfer of the Analog Voltage to Duty Cycle Generator project from the Westinghouse Molecular Electronics Division, West Coast Department, to the Westinghouse Research Laboratories, Information Devices Department, an analog implementation of the Duty Cycle Generator had been constructed in two forms; one a discrete component working breadboard model, and the other a model using integrated circuit components of the Westinghouse "Instacircuit" type together with some discrete components. As shown by the block diagram of Figure 17, this subsystem includes a reference supply, a difference amplifier, a triangle waveform generator consisting of a bistable element and an integrator, a comparator circuit, and an output circuit consisting of a binary element and power gates. The operating waveforms of this subsystem are shown in Figure 18, which shows how the output duty cycle changes with level of the amplified error voltage (i.e., with difference amplifier output). Also shown is a combined full-wave output obtained by shorting a control pin to ground.

The circuits for the several blocks are shown in Figures 19 through 22. The major difficulty in this version was the 0.05 μF integrating capacitor of the triangle generator, which, if made by tantalum film-tantalum oxide techniques yielding 0.6 pf per mil^2, would require 80,000 mil^2, i.e., an area measuring 400 mils by

200 mils. Later investigations showed that the integrating capacitor and resistor could be changed from 0.05 μF and 1000 ohms to 500 pf and 100 K with no linearity degradation at room temperature (see Figure 23). The values of these big integrating circuit components were finally fixed at .002 μF (requiring an 80 x 40 mil area) and 25 K as a compromise between large area requirements and stable performance over the required temperature range.

Further study and development of these circuits showed that the integrating circuit driver of Figure 21 could be omitted because of the much lower drive requirements of the 25 Kilohm integrating resistor. In addition, it was found that the 7-transistor balanced input integrating amplifier of Figure 21 could be replaced by the 4-transistor single-ended input amplifier of Figure 24, as the only effect of DC drift at this stage is to change the symmetry of the output triangular waveform, but does not affect the resultant duty cycle or operating frequency, as illustrated by Figure 25.

The circuits finally adopted for integration on silicon chips are shown in Figures 26 through 29. An evaluation of their behavior relative to the system specifications is presented in the following section.

2.3.3 Analysis of Circuit Performance and Specifications

2.3.3.1 Performance Specifications

The performance specifications for the analog voltage to duty cycle converter, originally dated 2/12/65 and amended 12/9/65, can be summarized as follows:

1. Repetition Rate: 2.5 KC $\pm$ 10%

2. Output Level (V_o, I_o):

   "1" level: $|I_o| \leqslant 5$ µA at $V_o = +20V$, $T = 75°C$

   "0" level: $V_o \leqslant 0.5V$ at $I_o = -50$ mA,
   $-10°C \leqslant T \leqslant 75°C$,
   $19V \leqslant V_s \leqslant 21V$

(3 and 4 are deleted by amendment of 12/9/65).

5. Supply Power (V_s):

   $V_s = 20$ V.D.C. $\pm$ 1V

6. Input Signal (V_i):

   V_i (center value) = 10V $\pm$ 0.01V

   Source Impedance = 10KΩ $\pm$ 5%

7. Circuit Sensitivity (C.S.):

Nominally C.S. = +1% duty cycle/-0.001 volt input.

Specifically, $\left|97\%-3\%/-0.05V-(+0.05V)\right| = 0.94\%/mV \leq \left|C.S.\right| \leq \left|97\%-3\%\ -0.036V - (+0.0360)\right| = 1.3\%/mV$

(Note: The high limit on sensitivity, 1.3%/mV, corresponds to a +3 db tolerance on circuit sensitivity agreed upon verbally by A. Schloss of Jet Propulsion Laboratory and P. Malmberg and M. Geisler of Westinghouse on 9/7/67.)

8. Output Linearity:

Duty cycle output vs voltage input linear within $\pm$ 2.5% between 3% and 97% duty cycle points.

9. Output Symmetry:

$(t_{ON})_A = (t_{ON})_B \pm 0.5\%$, and

$(t_{1/2})_A = (t_{1/2})_B \pm 0.25\%$,

where $(t_{ON})_{A,B}$ = "ON" time of A or B output, and $(t_{1/2})_{A,B} = \frac{1}{2}$ cycle period between the starts of the A and B "ON" times, or of the B and A "ON" times.

10. Temperature:

-10°C to +75°C

11. <u>Output Rise and Fall Time</u>:

$\leqslant$ 0.5 µS from "0" state to "1" state, or from "1" state to "0" state.

12. <u>Circuit Stability</u>:

If a given duty cycle = $X_1\%$, and $V_i(X_1\%)$ is the corresponding input voltage, then

$$V_i(X_1\%)_{max} - V_i(X_1\%)_{min} \leqslant 0.025 \text{ V for}$$

$$-10°C \leqslant T \leqslant +75°C \text{ and}$$

$$19V \leqslant V_s \leqslant 21V$$

2.3.3.2 <u>Circuit and Component Design as Related to Performance Specifications</u>

The planar silicon-tantalum film hybrid technology chosen to implement the voltage-duty cycle generator design offers the combination of integrated circuit compactness and reliability together with the temperature stability and precision of tantalum films. The present design uses several basic principles to meet the D.C. precision and temperature stability specifications listed in the preceding section. Perhaps the most significant of these is the use of resistance ratios to determine voltage levels and gains of feedback amplifiers. As shown in Table VI, this affords a stability in the determined quantity of about 20 ppm/°C for diffused resistors, or 2 ppm/°C for tantalum nitride resistors. A second principle used is the voltage stability of an adjoining pair of transistors used as a difference or comparing amplifier, yielding input stabilities of about 20 μV/°C or less. Another principle is the use of the tantalum nitride film resistors and tantalum capacitors where the highest temperature stability is required. Table VI lists the principle D.C. characteristics of the circuit components, together with their temperature coefficients.

The tantalum film technology offers a further significant advantage required in the present subsystem, namely the possibility of resistor trimming by an electrochemical micro-technique to an exact value, with an attainable precision of better than 0.1%. A major feature of the final design is the capability of trimming only one resistor in the assembled, mounted, and interconnected system to obtain a 50% duty cycle output for a center value input signal of 10V $\pm$ 0.01V (specification #6, preceding section). This resistor is one of the pair which determines the output level of the voltage reference source. By adjusting it after final assembly, compensation is obtained for D.C. offsets in the error amplifier, triangle generator and comparator. The other specifications are met by the component tolerances and tracking accuracies in the subsystem as fabricated, and do not require initial adjustment of the circuit component values.

A further understanding of how this is accomplished may be obtained by reference to Fig.30, which shows the D.C. levels and pertinent waveforms at various points in the subsystem together with their labels, and Table VII, which lists the various subcircuits and their contribution to subsystem performance.

The output rise and fall times are dependent on output transistor speed, including the effects of stored charge in the base region. The present design gives rise times of about 0.2 μs, well within the 0.5 μs specification limit. The output symmetry requirements (specification 9 of the preceding section) are easily met by the basic design of the subsystem, using as it does two alternating output channels which time share the same analog-duty cycle conversion channel and which are separately enabled by alternate whole cycles of the basic repetition rate source--the triangle waveform generator.

3. FABRICATION PROCEDURES

The design for the system having been finally determined as consisting of four monolithic blocks and a discrete thin film capacitor utilizing tantalum nitride and oxide components, the fabrication of these units could proceed.

The monolithic blocks are:

(a) Reference Supply
(b) Triangle Function Generator with Discrete Capacitor
(c) Difference Amplifier
(d) Digital Output

3.1 Tantalum Components

The use of tantalum thin film components in this system is dictated by the stringent requirements for resistor values and the large values of capacitance required for the triangle generator which would not be possible by conventional integrated circuit techniques.

A considerable amount of background work in analyzing the various methods of deposition of tantalum thin film components was carried out and this is reported in Appendix II. It was determined that the best control on resistor sheet resistance and minimum temperature dependence could be obtained using tantalum nitride as the resistor film.

3.1.1 Tantalum Nitride Resistors

Tantalum nitride resistors covered with anodically grown tantalum oxide exhibit high stability.[1] Such films are sputtered through deliberate addition of nitrogen to the argon sputtering gas. To fabricate the resistors and capacitors in a compatible manner with diffused silicon monolithic circuits, the following masking technique was developed: The diffused silicon wafers are covered with an aluminum rejection mask, the delineation of which is made by normal photoresist techniques. The mask has windows with the form of the required resistors. A film of tantalum is then sputtered reactively over the aluminum. After rejecting the aluminum mask a second aluminum layer is delineated applying photoresist technique. This mask leaves uncovered the areas of the tantalum nitride film which are to be anodized, but interconnects the resistors on the wafer. The tantalum nitride is then anodized along with the aluminum. The next step is to dissolve the aluminum Al_2O_3 mask. After evaporating a new aluminum layer, the actual interconnections are formed by photoetching as in normal metallization technique. Gerstenberg and Calbick[2] have shown that the specific resistivity of the sputtered nitride metallic compounds is a function of the partial nitrogen pressure during sputtering; a result which was confirmed by our experiments. Grown in a partial pressure of .4 micron of nitrogen, the films have a specific resistivity of 250 μΩcm. With the thickness of the resistor structure chosen at 1000 Å, the sheet resistance is 25 Ω/□, the temperature coefficient of resistance is 160 ppm/°C. Actually, the films are deposited to a thickness of 1250 Å. A 250 Å thick layer is then converted upon anodization to SiO_2. Following this, a 1000 Å Ta_2O_5 layer is grown. The oxide protects the resistors.

3.1.2 Thin Film Capacitors

Pinholes in either the silicon dioxide, the tantalum nitride or the tantalum pentoxide layer prevented integration of the large area capacitor into the triangle generator. The structure of the discrete capacitors consists of a TaN bottom electrode, a sputtered Ta_2O_5 dielectric and an aluminum top electrode. It is fabricated on a low resistivity silicon wafer. After scribing, the capacitor is mounted in a separate flat pack. The electrical characteristics are:

$C = 2000$ pF

$C/\text{mil}^2 = .62$ pF

$D = .002$ (loss tangent)

$\rho > 10^{15}\ \Omega$ cm

TCC = 160 ppm/°C

3.1.3 Assembly and Operation of a Triode Sputter System

A low pressure triode sputter system as devised by Spivak et al[3] was built up in a form quite similar to the system currently manufactured by CVC[4], except that instead of using a single coil to generate the magnetic field a Helmholtz coil configuration is utilized, resulting in a more uniform plasma in the target region. The sputtering system is shown in an overall view in Fig. 31; a close-up of the target-substrate-anode region in Fig. 32;and a schematic outline of the unit is given in Fig. 33. The incandescent filament acts as the electron source. Argon, admitted through a needle valve to maintain a partial pressure of 4 microns, is ionized and the resulting plasma sustained between the anode and the filament (cathode). The magnetic field of about 40 oersted constricts the plasma in the target-substrate region and enhances the ionization probability of the argon atoms. The target, which is negatively biased at 1500 volt, is immersed into the plasma. Species of the tantalum target are sputtered as a result of surface collisions between impinging ions and the target atoms. Sputtered in argon, tantalum films have a cubic bcc structure like the bulk material or a tetragonal structure[5] - so called β-tantalum not found in the bulk. Deliberate addition of a reactive gas, in our case nitrogen, produces metallic compounds with higher resistivities than tantalum.[2] We found that an addition of nitrogen at a partial pressure of .4 microns results in films with a specific resistivity of 250 μΩcm.

3.1.4 Anodization

Oxidation of the tantalum nitride films is performed in an aqueous electrolyte through anodization. The oxide grown in this manner forms the passivation layer on the resistors. After the circuits are assembled in the package, a second anodization to trim the precision resistors, is performed. Figure 34 is a schematic outline of the anodization facility. The anodization is carried out in two consecutive stages:

- anodization with a constant current until the voltage across the electrolytic cell reaches a predetermined value.
- this voltage is then held constant during the second mode and the current eventually decays.

The electrolyte utilized is a .02 percent aqueous solution of citric acid. The current density during the constant current anodization mode is fixed to 1 mA. To form an oxide layer of 1000 Å thickness, a voltage of 60 volt is required across the electrolytic cell. The final trimming of the precision resistors is performed through microanodization. The method of drop anodization was previously described by Maissel et al.[6] and is schematically depicted in Fig. 35. This anodization narrows the cross section of the resistor on which it is performed and consequently enhances the resistor value.

3.2 Integrated System Design

An initial design study, emphasizing power dissipation and stability, divided the system between six separate silicon chips.

By excluding the load resistors from the final output stage, it was possible to reduce the total power dissipation in the system from 2200 milliwatts to 880 milliwatts and this allowed the designs to be consolidated into four separate chips. These are: the reference supply, differential amplifier, triangle generator with discrete capacitor and output circuit. Furthermore, the layout of the four chips was organized such that a single chip unit can be made using a simple interconnection overlay mask in the event that four adjacent chips on the same slice are all functioning correctly.

A design layout for the complete AVDC system was made giving the relative position of each chip and fixing the paths of leads that must be made for interconnection. The overall layout of the system is shown in Figure 36. The design is somewhat conservative in allowing 50 mils distance between circuits. This can be reduced to approximately 5 mils in the one chip design. As shown, the final encapsulation must consist of a six terminal, package capable of dissipating the 900 mw produced in the overall circuit. The layout has been made such that a complete one-chip mask can be produced once the individual desired characteristics of each circuit have been obtained.

A final trimming operation on the overall system was set up in two steps to achieve the final output characteristics. First, the tantalum resistor associated with the triangle generator was to be trimmed by etching the resistor, while monitoring the generator frequency and obtaining 2.5 kc. The triangle generator, differential amplifier and output circuit could then be mounted on the ceramic substrate, leaving the reference supply unmounted. After it was determined what voltage was required to give the correct symmetry of inputs at the comparator amplifier, the reference supply could be trimmed to this voltage, then mounted in place in the AVDC system. When the single chip AVDC system is made, this operation can be made after the chip is mounted.

3.3 Reference Supply

The physical layout for the reference supply is shown in Fig. 37.

The substrate material was chosen to be 1Ω cm n-type epitaxial silicon approximately 25 microns thick. This material will yield transistors with a V_{CEO} of 25V, betas greater than 50 and saturation resistance less than 300Ω. Space for a tantalum resistor has been allowed on this chip which was deposited after the circuit had been checked for operation.

Since the zener diodes should have as near a zero temperature coefficient as possible, the diodes and transistor base regions were diffused with 200 Ω/□ sheet resistance to give 5.8V reference diodes.

Eight lots of four slices were processed for reference generators. The first six of these lots contained reference amplifiers which were fabricated with a diffused zener-linearity resistor. Two lots of these six produced units which functioned in the overall system but did not meet the regulation specification for this part of the system. In addition, these regulators could not be adjusted with external resistors to the desired 10V nominal voltage level required for the reference bias. These units operated at approximately 11V due to a 7V reference zener diode which should operate at 5.8V.

To alleviate the latter problem a seventh lot was diffused with a 2.4μ base depth rather than the 2.7μ depth previously used, which brought the zener voltage down to the specified level. An eighth lot is now being run using an alternate mask which will allow a tantalum resistor to be fabricated in place of the diffused one. This allows some adjustment in the zener current and should also improve regulation because of the improved thermal coefficient. A photograph of a completed unit with untrimmed resistors is shown in Figure 38.

3.4 Difference Amplifier

The layout for this circuit is shown in Figure 39. This amplifier is fabricated on the same substrate materials as used for the reference supply. In addition, floating collector regions are required because of the two zener voltage specifications

The circuit of the difference amplifier consists of two differential stages in series. The most difficult components to fabricate are:

a) A Zener diode of ∿8V, which is required for a voltage level shift between the two stages.

b) Three capacitors of the ac-compensation network which have to withstand a peak voltage of 10V.

Since the Zener voltage has to be smaller than the breakdown voltage of the capacitors, it is impossible to use one kind of junction for both.

The initial concept used reversed biased base-emitter junctions which give a high capacitance/unit area for the capacitors, with a breakdown voltage of 14 volt. The level-shifting Zener diode was made from a small emitter junction with the desired breakdown voltage. The first fabrication run revealed that it is difficult to control two junctions with different breakdown voltage simultaneously and at the same time to get the desired gain for the transistors. For this reason, several test runs were carried out first with the objective of achieving separately the desired small Zener diodes and the required base-emitter breakdown voltages. After these evaluations, the results were compiled and used in the procedure for subsequent circuit fabrication. A picture of the integrated circuit chip is shown in Fig. 40. Parallel to this effort, alternative solutions have been persued to circumvent the problem of controlling two junctions simultaneously. By changing from emitter-base junction capacitors to p wall diffusion-emitter capacitors, one has only to insure the breakdown voltage exceeds a specific value. This could also be achieved by the replacement of the junction capacitors by thin film capacitors.

Both alternatives need only one specific breakdown voltage; the first has the additional feature of being easier to fabricate.

A final eight wafers were run with the new masks which incorporates SiO_2 capacitors in place of the p-wall diffused type. This required some enlargement of the original areas but relaxed the specification requiring two critical breakdown voltages. The final mask change also incorporated an adjustment in the feedback network resistors to increase the overall amplifier gain, since this had been low in some of the earlier runs. Test results on these final wafers indicate rather low yields but high enough to supply the units for the final systems.

3.5 Triangle Generator

The layout for this chip is shown in Figure 41. This integrated circuit contains the .002 μf tantalum capacitor and 25K resistor which account for roughly 75% of the area of the chip. The triangle generator is fabricated on the same material as the other devices, but will not require a floating collector region under the epitaxial layer. The circuit contains a 14V reference diode requiring that the base of the transistors be fabricated with 250Ω/□ sheet resistance at a depth of 4 microns.

Four lots have been run for the triangle generator circuit with these slices all being rejected for low-transistor beta and, in some cases, low zener voltage. A fifth lot was processed for aluminum interconnects which contain transistors with betas of 25-30. Although these betas were still quite low, they were probed using an external resistor and capacitor in place of the tantalum components and tested for operation. A chip that does not as yet contain the tantalum components is shown in Figure 42.

Twelve wafers with betas of 50 or greater were processed for this particular circuit, four of these slices being processed with tantalum resistor and capacitor. However, due to pin-holing in the tantalum oxide dielectric, the capacitor showed shorts between the aluminum upper electrode and lower tantalum nitride. It was found that this condition was primarily due to the imperfect surface of the integrated circuit, since capacitors of high yield could be made on flat silicon with freshly grown oxide.

Due to this occurrence of capacitor shorts, it was decided to process the other eight wafers for tantalum nitride resistors only, then fabricate the capacitor on a separate piece of silicon. The yield of these circuits turned out to be approximately 5% before mounting in flat packages.

3.6 Output Circuit

The layout for this circuit is shown in Figure 43. Four slices which contained transistors with betas in the 25-30 range were probed before mounting and found to contain working units; however, the bistable multivibrator could not be triggered with the capacitor fabricated with the chip. An investigation was made of the capacitor which indicated that the capacitance was the correct value, but the series resistance associated with the capacitor was abnormally high. A curve of capacitance with respect to voltage is shown in Figure 44.

It was felt that this resistance, although generally high for this type of capacitor, would not be adequate for this application. Previous slice runs of this circuit had resulted in low yield for primarily two reasons. First, there was a capacitor junction breakdown problem in the multivibrator section of the circuit which was remedied by diffusing the lower plate of the capacitor during the boron isolation diffusion. The junction is required to support at least 15 volts before breakdown which is at least 5 volts above the regulating supply of the multivibrator circuit. Previously, these voltages were very close to each other leading to marginal operation of the circuit. The upper plate of the capacitor and the emitter of the zener diode are normally diffused at the same time.

Another step taken to increase the number of good circuits was to simply increase the number of available circuits on a slice by restepping the masks at smaller step and repeat distances. This can now be done because the chips are bonded into individual packages thus conserving silicon area previously required between circuits. The number of available circuits on a slice has now been increased by about 10% over the older design.

A complete set of chrome masks were also made when the new masks were re-stepped which lowered the pinhole density and increased edge acuity.

Three operable logic circuits have been obtained from the first low of four wafers. Sixteen other wafers were processed yielding enough circuits within specification for the required systems. A picture of the final integrated circuit chip is shown in Fig. 45.

3.7 Encapsulation

3.7.1 Interconnection Design

The utilization of the same circuit configurations for the four chip layout as for a monolithic design greatly simplifies the lead patterns required in the ceramic substrate of the package for the flip-chip assembly. All the lead terminations have a simple one to one correspondence with the related termination on the adjacent chip so that the intraconnection lead lengths are minimized and no cross-overs are required on the package, as is shown in the layout diagram of Figure 36.

3.7.2 Thermal Dissipation

The major design problem which arises with the use of a flip chip assembly technique is the thermal dissipation, which is limited in each chip, by the heat which can be removed via the interconnection pads. Since the total area of these pads is much less than the total chip area, the thermal resistance for the flip-chip configuration is higher than for a conventional back mounted chip. A comparative example for the differential amplifier chip, which has the highest power dissipation (300 mw) on the smallest area (80 mil x 75 mil) is given below.

Assuming the possibility of spacing 5 x 5 mil pads at 10 mil intervals for the flip-chip assembly, the maximum number of pads round the periphery is sixteen and the total pad area is 400 mils^2 compared with 6000 mils^2 for the total chip area. This reduction in effective heat conductive path together with the additional factor of the transmission of the heat to the pad within the chip itself leads to a working junction temperature of 131.5°C for an 85°C ambient in a worst case analysis for the flip-chip structure compared with a junction temperature of 101.3°C for an 85°C ambient if the chip is totally contacted. Thus, the improvement in reliability gained by avoiding the use of bonded wires in the flip-chip structure may be somewhat deteriorated by the higher junction temperature which may have to be tolerated.

Initial encapsulation of the system is therefore being carried out in separate flat packages for each chip in lieu of a single flat package using bonded leads.

4. CONCLUSIONS

This project for the fabrication of an Analog Voltage to Duty Cycle Generator in monolithic form has reached the point at which the final design has been made into integrated circuit form. Although the format for the layout of the system was designed so that a single monolithic chip could be obtained, it appears from considerations of power dissipation, operating temperature and yield that the best alternative for good reliability is four chips and a discrete thin film capacitor mounted into single flat packages.

The incorporation of tantalum oxide capacitors and tantalum nitride resistors into these circuits has allowed more stringent requirements to be placed on these component values than is normally found in integrated circuits. It is apparent that the use of such integrated thin film components in linear integrated circuits will allow greater freedom of design and improved performance.

Although good tantalum oxide capacitors were made on integrated triangle generators and likewise good triangle generators were also made, the yield was such that an operable triangle generator with a good capacitor could not be fabricated. This made it necessary to fabricate a discrete tantalum thin film capacitor with a good triangle generator containing a tantalum nitride resistor to get working systems.

Tests at -10°C and 75°C on the five AVDC systems indicate that one system meets all specifications other than for the input signal center value and symmetry specification. The other systems do not meet specifications for various other reasons. The failure of the #1 system to meet all specifications is due to a zener diode in the reference supply having a zener voltage approximately 0.5 volt above the desired value. The integrated circuit was originally designed so that this voltage could be adjusted to the proper value by trimming the tantalum resistor divider network. However, these resistors can only be changed by about 3% with this technique making it impossible to adjust the input signal center voltage the required 0.5 volt. This was the case for the reference supplies for all five systems.

A picture of the test fixture is shown in Fig. 46, the test procedures are included in Appendix III and the results of the tests on all five systems are shown in Table VIII. Also, a complete flow diagram of the fine packaged circuits is shown in Figure 47 showing pin positions, biases, and operating signals.

APPENDIX I

FREQUENCY STUDY OF THE REFERENCE SUPPLY

When integration of the 10-volt reference supply was considered, it was felt that by reducing the value of the shunting capacitor, the chip size could be reduced thereby increasing the yield.

An investigation of the effect of this shunting capacitor was therefore necessary. This investigation consisted of a loop gain analysis of the circuit. Assuming that the transit times of the transistors are negligible and neglecting the transistor input and output capacitance, the transfer function of the circuit can be given as

$$G_I = \frac{11 \cdot 10^2 \left[1 + j\frac{\omega}{\omega_1}\right]\left[1 - \left(\frac{\omega}{\omega_A'}\right)^2 + j\frac{2\delta\omega}{\omega_A'}\right]\left[1 - \left(\frac{\omega}{\omega_C}\right)^2 + j\frac{2\delta\omega}{\omega_C}\right]}{\left[1 - \left(\frac{\omega}{\omega_A}\right)^2 + j\frac{\omega 2\delta}{\omega_A}\right]\left[1 - \left(\frac{\omega}{\omega_E}\right)^2 + j\frac{2\delta\omega}{\omega_E}\right]\left[1 - \left(\frac{\omega}{\omega_H}\right)^2 + j\frac{2\delta\omega}{\omega_H}\right]}$$

where

$$\omega_1 = \frac{1}{r_e C_{eB}}$$

$$\omega_A' = \sqrt{\frac{1}{3750\ C_D C_Z}}$$

$$\omega_C = \sqrt{\frac{1}{48 R_L C_D[C_{BC}+C_L]+63R_L C_Z[C_{BC}+C_L]+C_D C_Z[610+.2R_L]+R_L r_e C_{EB} C_{CB}}}$$

$$\omega_A = \sqrt{\frac{2+0.03\beta}{C_D C_Z[750+3.8\beta]+20\beta C[88C_D+150C_Z]}}$$

$$\omega_E = \sqrt{\frac{6200+140K\beta R_L}{\begin{aligned}&6200[48C_D C_L(C_{BC}+C_L)+63C_Z R_L(C_{BC}+C_L)+\\&C_D C_Z(610+0.2R_L)+r_e R_L C_{EB} C_{CB}]+\\&\beta[C_D C_Z(140KR_L+r_e(25KR_L+85K^2)]+\\&r_e C_D R_L 10^3(6600C_L+6700C_{EB})+r_e R_L C_Z 10^3\\&(8700C_L+8800C_{EB})\end{aligned}}}$$

$$\omega_H = \sqrt{\frac{7400+R_L}{7400R_L C_L r_e[C_{EB}+C_{BC}]+r_e C_{EB} C_{CB} 7400 R_L}}$$

The Bode plot of this function is shown by the curves in Fig. 1A for two different values of shunting capacitance. From the plot it is seen that with $C = 0$, we have strong peaking in the 200 MC region, which is an indication of possible instability, leading to improper operation of the circuit. With a shunting capacitance value of 30 pf or larger, a lower break point is established, eliminating the peaking effect as shown by the upper curve of Figure 1A. A smaller value of C would yield a higher breakpoint which would not be as effective as the present one. Thus, the integrated circuit model was designed using the 30 pf value.

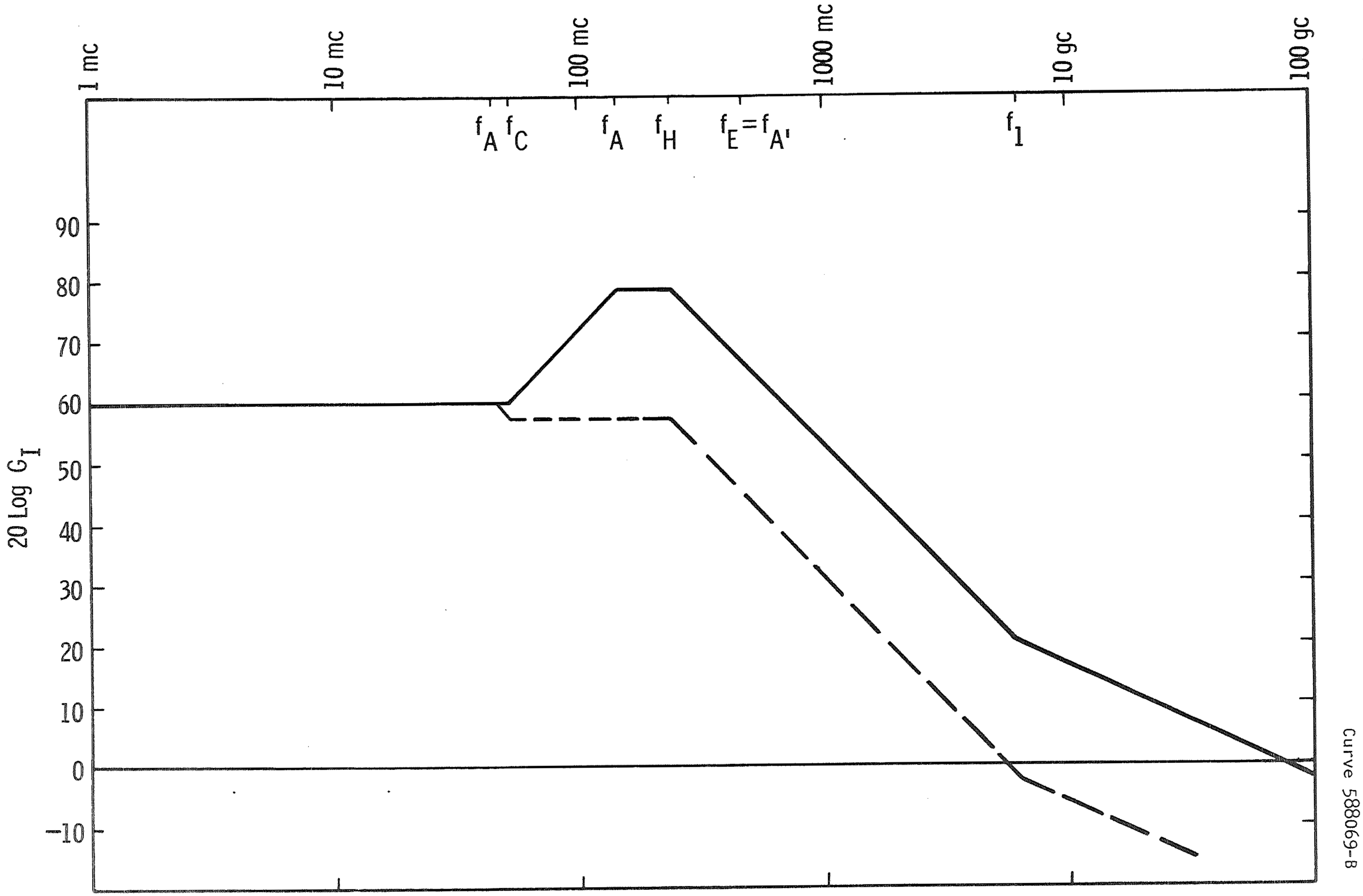

Fig. 1A—Bode plot

APPENDIX II

THIN FILM CHARACTERISTICS AND FABRICATION TECHNIQUES FOR TANTALUM FILMS IN INTEGRATED CIRCUITS

TABLE OF CONTENTS

Thin Film Characteristics and Fabrication Techniques for Tantalum Films in Integrated Circuits

I. Purpose of Report

The purpose of this report is four-fold: (1) to present information collected from current literature, (2) to state the duties completed, (3) to present and discuss data obtained from experiments conducted, and (4) to make suggestions. The topics are discussed, in the body of the report, as they are listed above. Information here represents the total amount obtained for the month beginning February 6th and ending March 3rd.

II. Film Fabrication

Tantalum films are to be used in forming the passive components of an integrated circuit currently being developed. Success in this endeavor will require that control be established over the deposition of the tantalum films as well as subsequent processing steps. Sections that follow discuss interdependent film characteristics and the resulting control required in each step of the film fabrication. The literature indicates that much work has been done with tantalum thin films and it has been found that sputtering conditions vary due to differences in pumping rates and geometries in each system. Because of this, even though much film information is presented here, a precise set of instructions cannot be written for the fabrication of a specific film component.

A. The Sputtering Process

The sputtering of a thin film occurs in the following manner.[10] A vacuum in the range of 10^{-3} or 10^{-2} torr is induced in the chamber. A voltage of a few KV, depending on the distance between the electrodes, is applied to the electrodes, the tantalum being made the cathode and the work table carrying the substrate the anode. This results in the ionization of the argon, forming a glow discharge. The argon ions are accelerated to the tantalum cathode and strike it with sufficient energy to remove tantalum atoms from the surface. These tantalum atoms then diffuse across to the substrate on the anode and form a strongly adhering film. Table 1 on page 57 is a chart of the various data for each of the sputters mentioned by the references.

It is of interest to note at this point that sputtering from a 13 inch diameter cathode gives a thickness uniformity of about $\pm$ 2% over a central 6 inch diameter area.[13] Others report that variations of only a few percent in resistivity over an area comparable to the cathode have been obtained.

1. Pure Tantalum Films

Films have been prepared with sheet resistivities of more than 700 $\Omega/\square$ and a temperature coefficient less than 100 ppm/$^{\circ}$C. However, the more usual values found in practice to give good stability are about 100-200 $\Omega/\square$ and 100-200 ppm/$^{\circ}$C respectively. The thickness of such films is about 100 Å. The stability of such films when heated in air is not very good, owing to progressive oxidation, and attempts have been made

Table I

SPUTTER DATA

Reference No. / Data	4	5	6	11	13	14	18	24	11
Type of Tantalum Deposit	Ta	Ta_2O_5	Ta and TaN	Ta	Ta	Ta	TaN	Ta	TaN
Initial Evacuation Pressure Chamber		5×10^{-5} torr	2×10^{-6} torr	10^{-5} torr	1×10^{-6} torr		5×10^{-4} torr		10^{-6} torr
Chamber Flush Mixture		50% Ar 50% O_2							
Presputter Time		15 min	20 min						
Sputtering Pressure	20μ	5×10^{-2} torr 50% Ar 50% O_2	1.5×10^{-2} torr	10^{-2} torr	5000 - 50000 $\frac{\text{millitorr-liter}}{\text{min}}$	50μ		40μ	$N_2\begin{cases}10^{-6} \text{ to} \\ 10^{-3} \text{ torr}\end{cases}$ $+10^{-2}$ Ar
Cathode Diameter					13 in.		3.3 cm		
Source-to-substrate Distance	2 in.	1 ± 1/4 in.					1-1/4 in.	1 in.	
Cathode-to-anode Voltage	5000V	1600V	5000V	1.5 KV		3000V	1500V	2800V	
Cathode-to-anode Current			20 ma						
Current Density	resistor-- dielectric--	5.0 mA/in^2 0.5 mA/in^2				1 ma/cm^2	6.6 ma/cm^2	1.67 ma/cm^2	
Film Deposition Rate			120 Å/min			10-18 Å/sec	60 Å/min		
Substrate water-cooled						yes			
Substrate temperature		25°C				temp. rise to 300°C			
Time of Sputter	60 min	45 min-resist. 180 min-diel.					20 min		
Resulting Film Thickness	5000 Å			500 Å			500 Å		

to improve this by incorporating gold doping and by nitriding during deposition.[11] Nitriding of the tantalum films will be discussed later.

Other methods of controlling growth processes are also important. Deposition of tantalum films at relatively low voltage but high argon pressure, i.e., 1-3 KV and 20-120 millitorr, results in films of 2000 $\mu\Omega$cm, i.e., 1000 $\Omega/\square$ for a 200 Å film, and essentially zero temperature coefficient. These films consist primarily of tantalum with exceptionally small crystallite size, possessing therefore a very small mean free path and a temperature coefficient relatively independent of the thermal lattice vibrations but constricted by grain boundaries. Attention to such important parameters as composition, structure, and deposition conditions of background pressure, electrode configuration, and materials of construction cannot be overemphasized in attempting to deposit films reproducibly for electronics applications.[13]

Gerstenberg and Mayer[6] give some interesting information, on tantalum thin films, in the form of a graph as seen in Fig. 1. Figure 1 illustrates the dependence of resistor stability on temperature coefficient and film thickness. These films were prepared under presumably identical conditions in the same vacuum system. However, at each film thickness a wide range of temperature coefficients with a dependent resistor stability can be observed. Generally, however, the stability increases with decreasing temperature coefficient and it may be concluded that there are particular vacuum conditions which produce films of exceptional stability.[6]

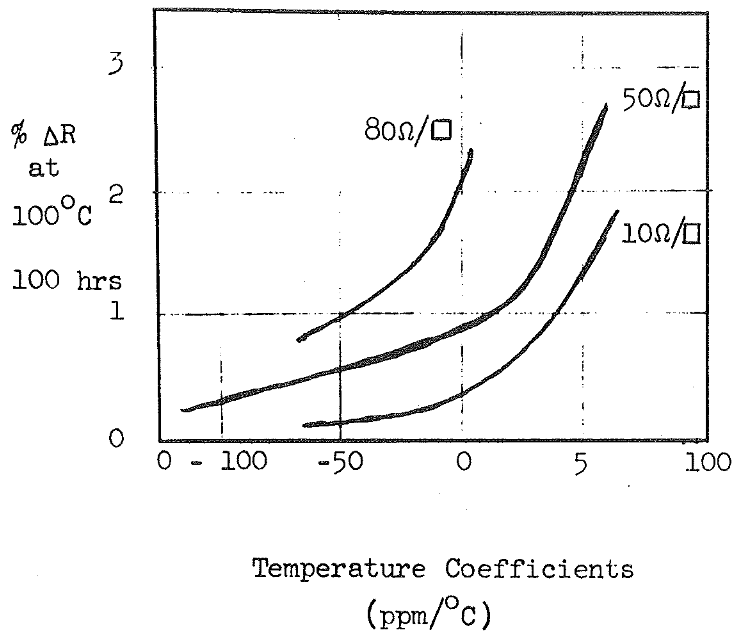

Fig. 1 The dependence of resistor stability on temperature coefficient and film thickness

2. Gold Doping of Tantalum Films

Stabilization of tantalum films can be obtained by the diffusion of gold into the tantalum film. One method of diffusion is to deposit a layer of gold over a tantalum layer and heat the films to 350°C in a vacuum. Schaible and Maissel[17,19] discuss the subject in more depth, but, for the purposes here, the comment by D.E.H. Jones[11] will suffice: "It has been proposed that the large increase in resistance of tantalum films, when heated in air, is due to the progressive oxidation along grain boundaries through the thickness of the film. This can proceed until oxide laminae penetrate right through to the substrate, and the film resistance increases by several orders when this condition arises. It has further been proposed that this oxidation process at the grain boundaries can be greatly reduced by the diffusion of gold along the boundaries. This is achieved by sputtering firstly a thin layer of tantalum, then a thin layer of gold and finally a thick layer of tantalum comprising the main part of the film. The gold is then diffused into the film by heating in vacuum to 350°C until diffusion is complete. The quantity of gold is critical, if too small the grain boundaries are only partially filled, resulting in unstable films, while if too much gold is present the film resistance is lowered by the undiffused gold. The optimum amount of gold is 7 percent by thickness. The films are then stabilized by heat treatment in air at 250°C to establish an oxide coating on the surface to protect it during its subsequent life.

Long-term stability tests on resistors which have been stabilized for 24 hours show a change of 0.5% after 400 hours at 150°C and the same change after 600 hours at 80°C and 99% relative humidity."[11]

3. Reactively Sputtered Ta_2O_5 Films

For reactively sputtered Ta_2O_5 films, a stable resistor film can be made, but the sheet resistivity is hard to control,[5] and the films possess undesirable high temperature coefficients as well as having measurable resistance fall-off at the frequency of only a few mc/sec.[13]

The reproducible control of reactively sputtered dielectric films is not yet adequately explored, but variables such as substrate surface, residual gas composition and sputtering current density probably are significant.[5] The sputtering conditions, used by Clark,[5] are given on page 63in Table 1.

For convenience, Tables 1 through 22 from Clark's report are given here. The tables are records of data under varying conditions for his Ta_2O_5 resistor and dielectric films. See page 68.

D. Gerstenberg and C. J. Calbick discuss the specific resistivity of Ta_2O_5 films as a function of partial oxygen pressure and show (on page 405 of their report) a graph of the relationship which is reproduced here in Fig. 2.

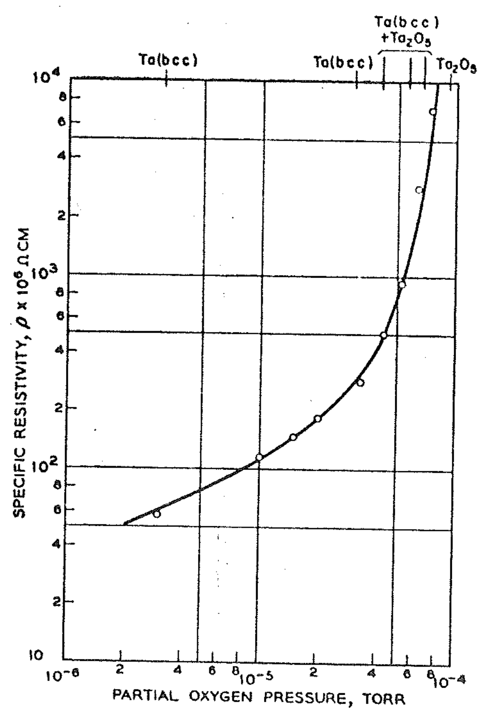

Fig. 2 The dependence of specific resistivity on oxygen partial pressure for Ta_2O_5 films

Table 2

Tables 1 thru 22 from Report No. 5
by R. Scott Clark and Coy D. Orr

Experimental Data on Ta_2O_5 Resistor
and Capacitor Films

Table 1. Resistance versus Temperature — Nominal 70 Ohms/Square Ta_2O_5/Ta Films

Lot	Ohms/ Square	Resistance, Ohms				
		+25°C	+125°C	+25°C	-55°C	+25°C
101	69	1,391	1,378	1,391	1,402	1,391
102	69	1,387	1,372	1,385	1,410	1,392
103	73	1,462	1,450	1,465	1,437	1,467
104	72	1,441	1,439	1,460	1,434	1,462
105	67	1,382	1,369	1,382	1,391	1,383

Table 2. Resistance versus Temperature — Nominal 500 Ohms/Square Ta_2O_5/Ta Films

Lot	Ohms/ Square	Resistance, Ohms				
		+25°C	+125°C	+25°C	-55°C	+25°C
111	624	6,242	6,109	6,243	6,363	6,243
112	826	8,258	8,065	8,243	8,432	8,259
113	298	2,980	2,926	2,980	3,030	2,990
114	436	4,369	4,266	4,361	4,450	4,362
115	827	9,085	9,000	9,090	9,120	9,100

Table 3. Resistance versus Temperature — Nominal 2000 Ohms/Square Ta_2O_5/Ta Films

Lot	Ohms/ Square	Resistance, Ohms				
		+25°C	+125°C	+25°C	-55°C	+25°C
065	2277	33,600	33,220	33,670	34,400	33,680
066	1427	14,269	13,908	14,265	14,611	14,262
067	2120	22,400	22,000	22,480	23,100	22,490
068	2948	35,600	33,890	35,780	36,700	35,790
069	1823	18,775	18,610	18,800	18,960	18,900

Table 4. Nominal 70 Ohms/square Reactively Sputtered Ta_2O_5/Ta Resistive Films

Lot	Ohms/ Square	TCR, ppm°/C -55°C to +125°C	After Heat Aging		
			24 hr 125°C %	2 hr 300°C %	TCR, ppm°/C -55°C to +125°C
101	69	- 96	+0.1	+11.2	- 80
102	69	-153	+0.3	+ 3.4	-140
103	73	-165	+0.1	+ 6.7	-160
104	72	- 96	+0.2	+15.3	- 87
105	67	- 59	+0.3	+ 5.9	- 43

Table 5. Nominal 500 Ohms/square
Reactively Sputtered Ta_2O_5/Ta Resistive Films

Lot	Ohms/ Square	TCR, ppm°/C -55°C to +125°C	After Heat Aging 24 hr 125°C %	2 hr 300°C %	TCR, ppm°/C -55°C to +125°C
111	624	-186	+1.0	+ 3.6	-143
112	826	-237	+1.3	+ 2.7	-216
113	298	-167	+1.4	+ 5.4	-152
114	436	-216	+1.6	+ 3.2	-187
115	827	-267	+1.7	+ 7.1	-248

Table 6. Nominal 2000 Ohms/square
Reactively Sputtered Ta_2O_5/Ta Resistive Films

Lot	Ohms/ Square	TCR, ppm°/C -55°C to +125°C	After Heat Aging 24 hr 125°C %	2 hr 300°C %	TCR, ppm/°C -55°C to +125°C
065	2277	-357	+3.7	+21.0	-327
066	1427	-327	+3.4	+20.6	-264
067	2120	-387	+3.8	+27.1	-362
068	2948	-423	+4.2	+25.3	-402
069	1823	-296	+5.6	+31.0	-281

Table 7. Temperature Cycling of Unprotected
Ta_2O_5/Ta Resistors

Lot	Ohms/ Square	Per Cent Change in R 25°C: After 24 hr. +125°C	After 2 hr. +300°C	After 15 min. +450°C
101	69	+0.3	+ 1.6	+ 5.6
102	69	+0.4	+ 2.1	+ 7.1
103	73	+0.5	+ 4.3	+ 8.3
104	72	+0.2	+ 3.1	+ 9.7
105	67	+0.1	+ 2.8	+ 8.3
111	624	+3.2	+ 6.3	+17.3
112	826	+2.7	+ 7.1	+28.4
113	298	+5.3	+ 5.3	+15.2
114	436	+4.2	+ 3.1	+16.3
115	827	+3.1	+ 4.8	+11.2
065	2277	+8.3	+11.2	+58.0
066	1427	+4.7	+ 8.2	+27.3
067	2120	+8.6	+ 9.7	+67.1
068	2948	+9.2	+13.0	+92.0
069	1823	+8.1	+11.2	+69.4

Table 8. Load Life Tests, 2 watts/inch^2, 125°C, Ta_2O_5/Ta Resistors

Ohms/ Square	R, 25°C, Ohms		
	0 Hrs.	1000 Hrs.	% Change
39	781	781	0.0
104	2,116	2,107	-0.4
206	4,195	4,220	+0.6
314	7,377	7,367	+0.1
511	10,579	10,936	+3.4
564	11,971	11,793	-1.5
756	18,383	17,692	-3.8
842	19,827	19,527	-1.5
912	18,672	18,664	0.0

Table 9. Results of Various Sputtering Times Reactively Sputtered Ta_2O_5/Ta Resistive Films

Lot	Process Variable	Results				
	Sputtering Time, Minutes	Ohms/ Square	Thickness Å	Å/ Minute	TCR ppm/°C	% Change After 2 hr 300°C
101-1	15	619	4,040	269	- 211	+ 8.1
101-2	30	237	8,890	296	- 197	+ 8.1
101-3	45	69	12,700	282	- 96	+11.2
101-4	60	54	16,500	275	- 15	+21.5
101-5	75	37	19,100	254	- 8	+10.0

Table 10. Results of Various Cathode Current Densities Reactively Sputtered Ta_2O_5/Ta Resistive Films

Lot	Process Variable	Results				
	Cathode Current Density mA/inch^2	Ohms/ Square	Thickness Å	Å/ Minute	TCR ppm/°C	% Change After 2 hr 300°C
102-1	1.0	175	4,900	109	- 172	+ 2.8
102-2	3.0	152	7,200	160	- 191	+ 4.3
102-3	4.0	112	8,400	187	- 156	+ 4.8
102-4	5.0	69	10,700	238	- 153	+ 3.4
102-5	7.0	27	14,800	329	- 21	+11.7

Table 11. Results of Various Oxygen Flow Rates Reactively Sputtered Ta_2O_5/Ta Resistive Films

Lot	Process Variable Flow Rate of 1% O_2 99% A 5 Scale = 2770 ppm	Results				
		Ohms/ Square	Thickness Å	Å/ Minute	TCR ppm/°C	% Change After 2 hr 300°C
103-1	1 Scale	28	13,700	304	- 20	+ 5.1
103-2	3 Scale	57	12,850	286	- 140	+ 4.8
103-3	5 Scale	73	11,690	260	- 165	+ 6.7
103-4	7 Scale	2,145	10,870	264	- 327	+ 9.3
103-5	9 Scale	25,400	10,630	259	-1280	+21.7

Table 12. Results of Various Chamber Pressures Reactively Sputtered Ta_2O_5/Ta Resistive Films

Lot	Process Variable Chamber Pressure, Torr	Results				
		Ohms/ Square	Thickness Å	Å/ Minute	TCR ppm/°C	% Change After 2 hr 300°C
104-1	1×10^{-2}	79	9,870	220	- 132	+ 5.8
104-2	3×10^{-2}	73	10,300	229	- 129	+11.3
104-3	5×10^{-2}	72	10,900	242	- 96	+15.3
104-4	7×10^{-2}	60	11,780	262	- 18	0.0
104-5	9×10^{-2}	29	13,200	294	- 3	+11.0

Table 13. Results of Various Substrate Temperatures Reactively Sputtered Ta_2O_5/Ta Resistive Films

Lot	Process Variable Substrate Temperature, °C	Results				
		Ohms/ Square	Thickness Å	Å/ Minute	TCR ppm/°C	% Change After 2 hr 300°C
105-1	25	67	12,100	269	- 59	+ 8.3
105-2	75	97	12,500	278	- 163	+10.2
105-3	125	167	11,650	259	- 197	+11.3
105-4	175	953	11,850	264	- 391	+13.7
105-5	225	2,948	11,980	266	- 547	+18.4

Table 14. Data for Capacitors During Assembly

Lot	pF/ mil^2	Probe Test		After Bonding		After Varnish Cure		After Canning	
		C, pF	Df	C, pF	Df	C, pF	Df	C, pF	Df
121-1	1.02	1623	0.010	1620	0.008	1612	0.003	1608	0.003
121-2	0.54	855	0.010	853	0.007	849	0.005	843	0.005
121-3	0.45	715	0.012	713	0.008	710	0.007	702	0.006
121-4	0.38	615	0.013	611	0.009	608	0.005	602	0.005
121-5	0.30	490	0.011	487	0.006	485	0.003	480	0.003

Table 15. Capacitance versus Temperature
Reactively Sputtered Ta_2O_5 Capacitors

Lot	pF/ mil^2	V_{bd}	Capacitance, pF at Various Temperatures +25°C	+125°C	+25°C	-55°C	+25°C	TCC, ppm/°C
121-1	1.02	25	1608	1646	1615	1582	1615	+218
121-2	0.54	33	843	854	843	834	843	+132
121-3	0.45	47	702	731	702	697	702	+269
121-4	0.38	68	602	610	602	596	602	+129
121-5	0.30	82	480	492	479	470	481	+253

Table 16. Temperature Cycling of <u>Unprotected</u> Ta_2O_5 Capacitors

Lot	pF/ mil^2	Percent Change After Storage					
		24 hrs 125°C		2 hrs 300°C		15 min 450°C	
		C	Df	C	Df	C	Df
121-1	1.02	+0.1	+8	+1.5	+9	- Shorted -	
121-2	0.54	+0.2	+8	+1.8	+8	+1.7	+27
121-3	0.45	+0.3	+7	+2.9	+6	+3.1	+18
121-4	0.38	+0.1	+6	+2.1	+3	+2.7	+13
121-5	0.30	+0.1	+4	+1.3	+2	+2.9	+ 7

Table 17. Life Test +125°C at 60% of V_{bd}
Reactively Sputtered Tantalum Oxide Capacitors

pF/mils^2	V Test D.C.	Measured at 25°C, 0.6 vac pp 1 Kc O D.C. Bias			
		0 Hours		1000 Hours	
		C, pF	Df	C, pF	Df
2.61	4	4957	0.018	4926	0.023
2.32	6	3673	0.017	3665	0.023
1.54	10	2742	0.006	2727	0.022
1.20	12	2008	0.007	1998	0.024
1.00	15	1551	0.008	1539	0.025

Table 18. Results of Various Sputtering Times
Reactively Sputtered Ta_2O_5 Dielectric Films

Lot	Process Variable Sputtering Time, Minutes	Results pF/ mil^2	Thickness Å	Å/ Minute	V_{bd}	Volts/ Å
106-1	60	1.76	585	9.7	6	0.013
106-2	120	1.41	900	7.5	10	0.011
106-3	180	0.97	1110	6.2	18	0.016
106-4	240	0.75	1390	5.8	20	0.014
106-5	300	0.56	1679	5.6	25	0.015

Table 19. Results of Various Cathode Current Densities Reactively Sputtered Ta_2O_5 Dielectric Films

Lot	Process Variable Cathode Current Density, mA/inch^2	Results pF/mil^2	Thickness Å	Å/Minute	V_{bd}	Volts/Å
107-1	0.125	3.16	500	2.8	8	0.016
107-2	0.25	2.13	560	3.1	17	0.030
107-3	0.50	0.98	1020	5.7	30	0.029
107-4	0.625	0.72	1200	6.7	35	0.029
107-5	0.75	0.64	1300	7.2	45	0.035

Table 20. Results of Various Gas Flow Rates Reactively Sputtered Ta_2O_5 Dielectric Films

Lot	Process Variable Flow Rate of 50% O_2 50% A 10 Scale = 2.38 SCFH	Results pF/mil^2	Thickness Å	Å/Minute	V_{bd}	Volts/Å
108-1	5 Scale	1.11	1100	6.1	25	0.023
108-2	6.25 Scale	0.93	1310	7.3	35	0.027
108-3	7.5 Scale	1.05	1285	7.1	35	0.027
108-4	8.75 Scale	0.98	1320	7.3	45	0.034
108-5	10 Scale	0.95	1270	7.1	50	0.039

Table 21. Results of Various Chamber Pressures Reactively Sputtered Ta_2O_5 Dielectric Films

Lot	Process Variable Chamber Pressure, Torr	Results pF/mil^2	Thickness Å	Å/Minute	V_{bd}	Volts/Å
109-1	1×10^{-2}	1.88	960	5.3	45	0.047
109-2	3×10^{-2}	1.13	985	5.5	35	0.036
109-3	5×10^{-2}	1.06	1050	5.8	25	0.024
109-4	7×10^{-2}	1.00	1170	6.5	15	0.013
109-5	9×10^{-2}	0.95	1200	6.7	10	0.008

Table 22. Results of Various Substrate Temperatures Reactively Sputtered Ta_2O_5 Dielectric Films

Lot	Process Variable Substrate Temperature, °C	Results pF/mil^2	Thickness Å	Å/Minute	V_{bd}	Volts/Å
110-1	25	1.00	1120	6.2	22	0.020
110-2	75	0.97	1165	6.5	25	0.021
110-3	125	0.93	1087	6.0	30	0.028
110-4	175	1.02	1130	6.3	35	0.031
110-5	225	1.12	1030	5.7	35	0.033

This completes all of the information that was found on reactively sputtered Ta_2O_5 films. However, Newton Schwartz references three other authors who have studied the preparation of tantalum oxide dielectric films by reactively sputtering for capacitors." These authors and their reports are listed below.*

(a) Anodically Grown Oxides

Although more will be said about anodic oxide films in the section on anodization, the following comment provides information on general film fabrication. Clark[5] states: "The use of anodic oxide films on tantalum for thin dielectrics is well known. Three properties have restricted their extensive use in conjunction with planar silicon active devices: the need to make ohmic contact to the tantalum during electrolytic formation of the dielectric; the adverse effects on silicon surfaces in electrochemical processing; and serious degradation during the temperature cycling normally used to contact and mount silicon devices. Reactively sputtered dielectric films were extensively studied, and show promise as a valuable material for thin film capacitors." No background data is given in the report to support his statements; however, he is the only one of the references cited (excluding the Westinghouse reports) who used silicon as a substrate. Further inquiry appears to be necessary.

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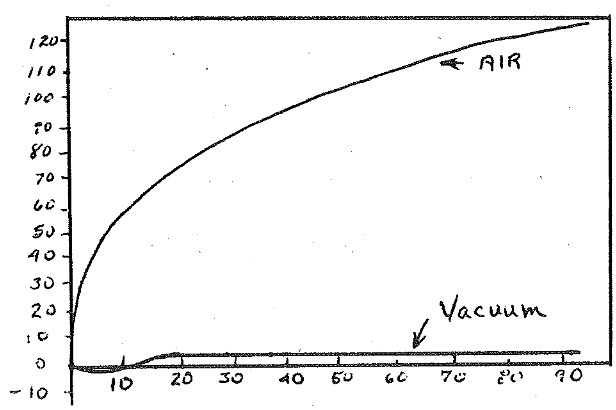
* Lane, C.H., Proc., Natl. Electronics Conf., 20, 1221, 1964.

Lloyd, P., Solid-State Electron., 3, 74, 1961.

Vrathy, F., The American Ceramic Society Meeting, Washington, D.C., May 1966.

(b) Oxides Grown in Heated Atmospheres

"High resistivity tantalum films have been prepared by sputtering in argon at low sputtering voltages. It is claimed that a 2 decade change in resistivity is obtained with about 2-1/2 times the change in sputtering voltage. Sheet resistivities of 4000 $\Omega/\square$ have been obtained with a film thickness of 500 Å when using a sputtering voltage of 1.5 KV. These films after anodizing and stabilizing in air at 200°C for 25 hours, showed good stability, subsequent change in resistance being less than 1% after 1000 hours at 100°C. These films have a negative temperature coefficient of -150 ppm/°C."[11] Jones' statement not only provides information on thermally grown oxides but includes in addition a new set of sputtering conditions. Jones[11] also states that resistance values can be readily controlled to ± 3% and, with care, adjusted to ± 0.02%. Maissel[14] also presents some data, in graphical form, for tantalum films heated at 250°C. These films had not been preanodized. This graph is shown in Fig. 3.



$\frac{\Delta R}{R}$ %

Time in hours

Fig. 3 Tantalum film stability dependence on time in heated oxygen atmosphere

4. Reactively Sputtered TaN Films

Most of the recent work on tantalum films has been directed to the reactive sputtering of tantalum and nitrogen. The reason for this action is that preliminary test results indicate that tantalum nitride thin films can be readily applied to the fabrication of resistors which have a high degree of reliability and stability, and can be commercially manufactured.[3]

As was mentioned earlier, of critical importance to the deposition of tantalum thin films is the reproducibility of the sputtering process. McLean has done some detailed work on the change of temperature coefficient, change in resistance, and change in resistivity of tantalum thin films as a function of the partial pressure of nitrogen during the sputtering process. Figure 4 is a graph showing the relationship of these functions. McLean calls Fig. 4 a calibration curve for a particular sputtering system.

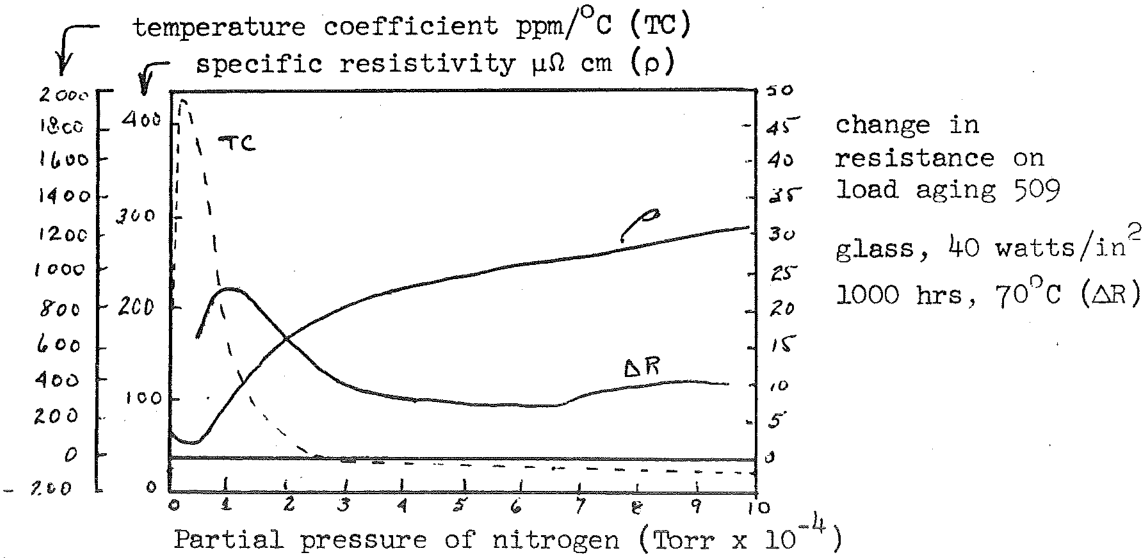
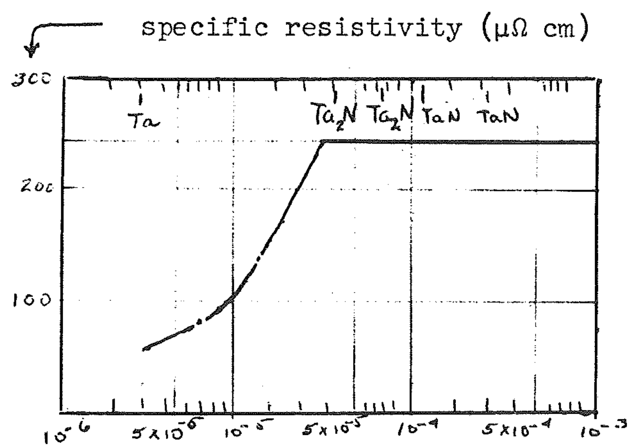
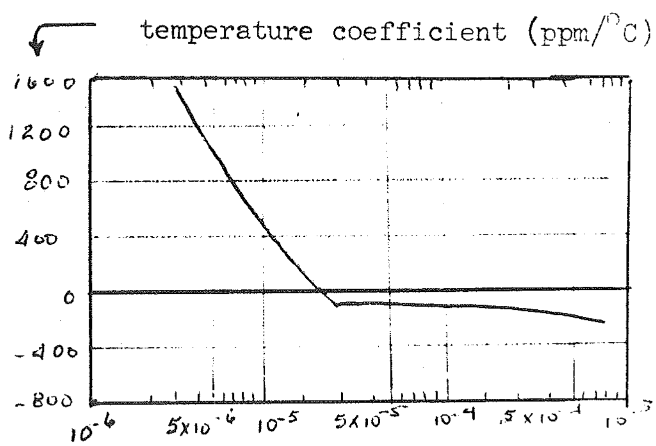


Fig. 4 The dependence of temperature coefficient, resistivity and change in resistance of TaN films on the partial pressure of nitrogen

Curves such as these permit one to choose an operating point consistent with product requirements.[23] In doing nitrogen doping experiments in a number of systems, it has been observed that the characteristic curves, as typified in Fig. 4, for one sputtering system, vary from system to system. However, at the optimum stability point, the film properties are always similar, with a composition of Ta_2N and TaN, a resistivity of about 250 μΩcm and a temperature coefficient equal to -50 to -100 ppm/°C.[11-12]

Gerstenberg and Mayer[6] show similar results for the specific resistivity over a wider range of nitrogen partial pressures. These results are shown in graphical form of Fig. 5. The relationship between temperature coefficient and nitrogen partial pressure is also shown in the same figure.





Partial pressure of Nitrogen
(mm Hg)

Fig. 5 The dependence of specific resistivity and temperature coefficients on the partial pressure of nitrogen

Similar to McLean, Gerstenberg states that "experience while reproducing the shape of the curve in another vacuum system has shown that the pressure at which the formation of the nitride starts might vary, depending on the pumping speed of the system, the sputtering rate and the size of the electrode. However, it is always possible to find a satisfactory operating point in any quality system through proper calibration."(6)

"The addition of nitrogen to the tantalum deposits is seen to result in significant improvements -- but perhaps most important is that the films produced at a carefully selected operating point are much more reproducible than those produced without doping."(12)

(a) Nitride Grown in Heated Atmospheres

There, like the oxidizing of the tantalum films, are two ways in which tantalum films can be nitrided: (1) by reactive sputtering and (2) by exposing the films to a nitrogen atmosphere at high temperatures. From page 3 of the Westinghouse Memo No. 66-9005-81-M2, resistors of tantalum films were stabilized by aluminum contact sintering in a travelling oven at 350°C and then thermally cycled in nitrogen at 450°C. "By carefully controlling the time in the nitrogen furnace, it is possible to adjust resistors to their specified values (2500 Ω/ □).(25)

(b) Combination Oxygen-Nitrogen Dielectrics

John Stringer(24) has written a report on "The Effect of Nitrogen on the Oxidation of Tantalum at High Temperatures." Here tantalum films are exposed to various ratios of oxygen-nitrogen atmospheres. The effect is the same -- or nearly the same -- as anodizing a tantalum nitride film.

Stringer found that oxidation in pure oxygen follows a linear rate law but the addition of nitrogen causes the reaction to become non-linear. He then discusses the results in terms of existing kinetic models. His was the only information obtained on this approach.

B. The Anodizing Process

The anodizing process is a common technique known to the industry for many years. Yet anodization of tantalum films is relatively new since there are many electrolytes and different electronic setups being used. Anodization is particularly applicable to tantalum thin films since it can be used for adjustment to particular values within a few tenths of a percent while at the same time providing an integral protective coat.[6]

The Westinghouse report[26] mentions using a .01% by weight agitated bath of H_2SO_4 at room temperature. The circuit used is a constant current-constant voltage type which will be discussed in more detail in the experimental section.

1. Tantalum Nitride Resistors and Capacitors

Tantalum nitride films can be anodized. The resulting surface film is a form of anodic tantalum oxynitride which grows gradually and with a very uniform thickness. The reduction in resistor thickness is 4.0 to 4.5 Å/volt and can be controlled to about ± 0.5 Å. Using automatic monitoring equipment, routine trimming of individual resistors is possible to 0.1%. By using very low current densities during anodization, a precision of ± 0.02% is attainable. Mass trimming of many resistors on a single substrate, while monitoring only one, is limited by the original uniformity of the film and the pattern geometry to about ± 3%.[8]

Gerstenberg and Mayer have improved the stabilizing of tantalum nitride films by anodization. Using the 0.20% citric acid electrolyte the nitride film was reduced by 4 Å/volt.[6,19] Resistors of 1000 Å thickness were stabilized by anodizing to 30 volts followed by heat treatment in air at 250°C for 5 hours. The resultant resistors showed a resistance change of less than 0.15% after 1000 hours at 150°C.[25] Table 3 gives resistance, anodization voltage and thickness decrease for various TaN film thicknesses.

The film thickness decrease for tantalum films 1000 Å thick was 7.5 Å/volt in the same citric acid electrolyte.[6,13]

Table 3

ANODIZATION INFORMATION FOR TaN FILMS

Film Thickness (Å)	Resistance (Ω/ □)	Anodization Voltage (volts)	Film Thickness Decrease (Å/volt)
1000	22.50	30	4.0
1000	25.10	45	3.2
1000	25.00	60	3.9
1000	23.30	75	4.2
750	30.50	30	4.0
500	51.60	30	4.6

Instead of forming an oxynitride film by anodization, Gerstenberg[6] has done work with heat treating to form a combination oxygen-nitrogen film. He reports that the resistors with a film thickness of 1200 Å had a resistivity of 22 Ω/□ and were stabilized at 400°C in air for an hour and were tested for 1000 hours at 150°C. The changes in resistance for the individual resistors on the three slides during the life test were -0.002 and +0.09%. The change in resistance during stabilization was not more than 10% and the temperature coefficient remained constant at approximately -60 ± 5 ppm/°C.

The only report that comments on tantalum nitride for use in capacitors is the one by McLean.[13] Even there his comments are vague. He presents a graph, which is shown in Fig. 6 and explains that "the negative slope portion represents a poor quality oxide film which has a low breakdown voltage in both directions."

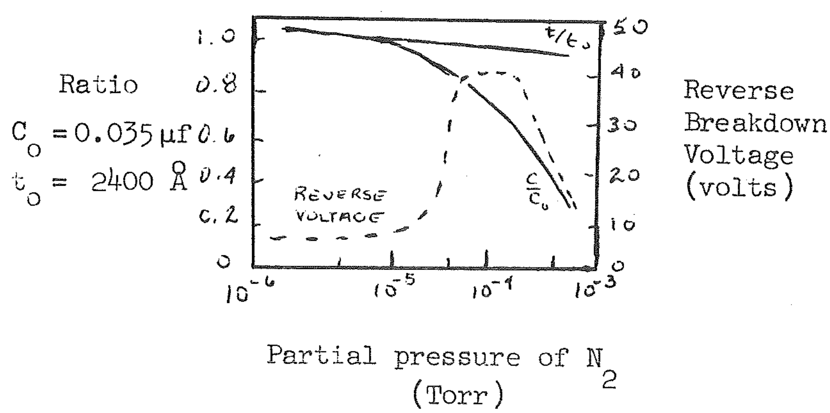


Fig. 6 Characteristics of TaN capacitors

In general, the field of tantalum nitride resistors looks very promising. Aside from good film characteristics, Berry[3] states that these resistors can be manufactured commercially to a high degree of initial precision (> ± 0.1%) and with a twenty-year lifetime stability under normal ambient conditions.

2. Thin Film Tantalum Capacitors

A platinum cathode is used with a typical electrolyte made of 0.02% citric acid, which gives a reduction in film thickness of 7.5 Å/volt. The oxide film obtained at a forming voltage of 100 volts has a capacity of 0.1 $\mu f/cm^2$, a dielectric strength of 5×10^6 V/cm and a temperature coefficient of 250 ppm/^{o}C. Sikina has used an electrolyte made from one part oxalic acid, 2 parts water, and three parts ethylene glycol. In this solution the Ta_2O_5 grows at a rate of 25 Å/volt so that a film formed at 100 volts is about 2500 Å thick. [6,9]

At Bell Labs. 1200 0.01µf tantalum capacitors were prepared by anodizing at 130 volts at room temperature and then evaporating on gold electrodes. Ninety percent of the capacitors had leakages less than 10^{-8} amperes and ninety-seven percent had less than 10^{-7} leakage current at 75 volts (dc), after a one minute of test voltage. Only 1.5% would not withstand the 75 volt test. These yields are just tolerable for thin film integrated circuits which have many capacitors per substrate. [13]

Berry and Sloan[4] give a table (see Table 4) of formation voltages and resultant capacitances. The electrodes were 250 mils in diameter.

Table 4

ANODIZING VOLTAGES FOR TANTALUM CAPACITORS

Formation Voltage (volts)	Capacitance ($\mu\mu f$)
5	250,000
10	185,000
20	92,000
40	68,000
100	30,000
150	20,000
200	15,000

As is seen from this table, the capacitance values, above 50 volts formation, are inversely proportional to the formation voltage.

C. A Comment on Etching Processes

The Westinghouse memo[25,23] mentions a one part HF, one part HNO_3 and two parts H_2O etching solution for tantalum. The only other etching solution mentioned among the references[5] listed was one for Ta_2O_5 and tantalum. The solution ingredients are:

3 parts by volume 48% HF

1 part by volume 70% HNO_3

3-20 parts by volume 98% acetic acid.

This solution was used on one Ta/Ta_2O_5 film in set No. 3. The etch was slow initially but needs close supervision since it is quite rapid once through the tantalum oxide film.

D. The Capacitor Counter Electrode

McLean, Schwartz and Tidd[13] have provided experimental results showing that the type of material used as the counter electrode in a Ta/Ta_2O_5 capacitor affects its breakdown voltage. This data is presented below in Table 5.

Table 5

THE EFFECT OF VARIOUS METALS AS COUNTER ELECTRODES ON THE BREAKDOWN VOLTAGE OF Ta/Ta_2O_5 CAPACITORS

Metal	Deposit	Anodic BDV (volts)
Gold	evaporated	91
Palladium	"	90
Copper	"	80
Antimony	"	75
Cadmium	"	71
Iron	"	45
Indium	"	41
Aluminum	"	24
Tantalum	sputtered	15

Berry and Sloan[3] reported that they used both gold and aluminum and no difference in breakdown voltages was observed. However, no data is presented.

In another of Berry's reports,[4] he includes the following pertinent paragraph: "Although the capacitors produced were essentially nonpolar, their leakages were higher than the reverse leakages on the non-symmetrical units. It is believed that the sputtering process used in applying the tantalum counter electrode may have injured the oxide film, since the same high leakages are observed if a gold counter electrode be sputtered instead of evaporated."

E. The Use of Aluminum instead of Resist

In the fabrication of thin film components the technique of obtaining the component patterns plays a central role. The patterns may be obtained using metal masks on the substrate during deposition or by using photolithographic techniques. The photolithographic process uses photosensitive chemicals - photoresists - applied to the surface in question. When light is allowed to pass through masks onto the treated surface, the resist emulsifies and protects the surface underneath from etches, anodizes, or further treatments. When the desired process is completed, the resist is then removed, leaving behind the desired film pattern.

As can be seen from the data presented in part V of this report, the photoresist is not withstanding the etch and the anodize processes. It is for this reason two additional methods, both using aluminum instead of photoresist, are mentioned here. McLean, Schwartz, and Tidd[12,13] describe these methods as a way to circumvent the resist breakdown problem. "In either case, aluminum is deposited over the tantalum coated substrate. Next, using a selective etch with photolithographic techniques, aluminum is removed from the resistor areas. Then an electrolyte suitable for both tantalum and aluminum is used and the whole sheet is anodized. Provided the aluminum has been deposited in sufficient thickness so that it does not anodize through, it may now be removed with a mild etchant leaving the bare tantalum in the desired pattern.

For the second method, more tantalum than needed is sputtered and is then covered with aluminum. By selective etch the resistor patterns of tantalum are exposed. Anodizing to some modest potential, say 25 volts, while using a compatible electrolyte covers the tantalum with an oxide film. A mild etch will then remove the aluminum. Finally, a fluoride etch is used and the oxide acts as a resist, preventing attack on the resistor area."

Most of the references do not mention a particular resist for use with the tantalum films. The Westinghouse memo,(25) however, mentions the use of AZ-340. Sikina(22) used KMER and KPR.

F. Methods of Fabrication of Resistor-Capacitor Patterns

Sikina(28) mentions a method for a resistor-capacitor fabrication. His report also has some pertinent life-test information on the tantalum thin film components. The procedure he mentions is as follows: "In addition to depositing the Au-Ta film, it sometimes may be convenient to deposit the dielectric for the capacitors by reactive sputtering techniques. KMER also can be used but the definition is poorer than with KPR."(22)

Comment

This concludes the correlation of data from the references listed. As the project matures, it is very likely that many new questions will arise which are not answered here -- especially in the testing phase of the components. However, it is hoped that the information supplied will be sufficient for present needs.

Table 6

A COMPONENT FABRICATION SEQUENCE

Step No.	Procedure
1	Deposit Au-Ta on substrate.
2	Apply KPR pattern over resistor and capacitor areas and develop the pattern.
3	Etch off excess Au-Ta to form the resistor-capacitor patterns.
4	Re-apply KPR and re-etch gold to complete its removal in the resistor-capacitor areas.
5	Stabilize tantalum resistors at 250°C for 5 hours.
6	Anodize capacitor areas.
7	Evaporate counter electrode.

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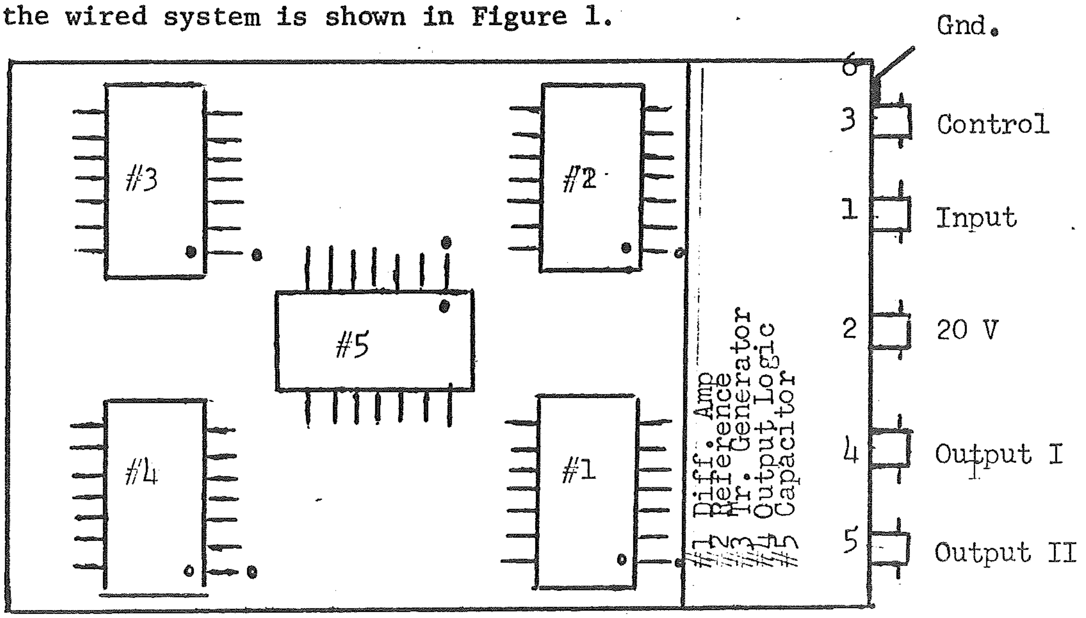
APPENDIX III

Test Procedures for the Analog Voltage to Duty Cycle Generator

1.0 The following test procedures are developed to demonstrate that the Analog Voltage to Duty Cycle (AVDC) generators meet the requirements of Engineering Note No. 342-50 and the subsequent modifications.

Each AVDC generator consists of four integrated circuits and a capacitor mounted in 14 lead flat packages. Functionally, they are a differential amplifier, reference, triangle generator, output logic and capacitor. The five packages are assembled into a complete AVDC system in a fixture supplied for testing. The fixture is completely labeled to show all inputs, outputs and power connections. The layout of the fixture, orientation of flat packages and schematic diagram of the wired system is shown in Figure 1.



Test Fixture For AVDC System

Fig. 1

2.0 For the following test procedures, pin 2 is +20 VDC and pin 6 is at ground potential.

3.0 Test Procedures. All procedures will be made at both -10°C and 75°C temperatures.

3.1 Repetition Rate

3.1.1 Required Equipment: Tektronic 545 oscilloscope, Leeds & Northrup .1% potentiometer, DC VTVM.

3.1.2 Connect a DC VTVM capable of reading 100 mv between terminals T_1 and T_2 as shown in Figure 2. Adjust R_4 for 100 mv on V_1 and set R_2 at midscale.

3.1.3 Connect the AVDC generator as shown in Figure 2 and adjust R_5 for 50% duty cycle on the oscilloscope waveform. Measure the time of one full period of cycle time.

3.1.4 Specified period should be 400 μsec ± 40.

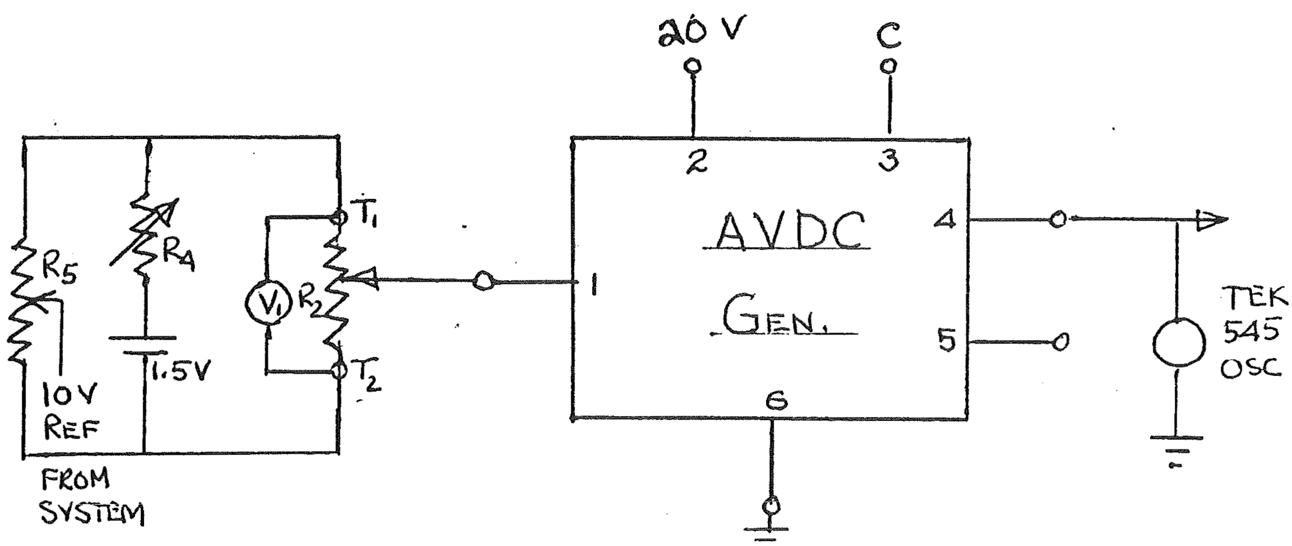


Fig. 2

3.2 Output Level

3.2.1 Required Equipment: Tektronix 545 oscilloscope, DC VTVM, Tektronix P6016 AC Current Probe, 0-10 μa ammeter, .1% Leeds & Northrup Potentiometer.

3.2.2 Connect the AVDC generator as shown in Figure 3.

3.2.3 Measurement Procedure. 1" Level. Read ammeter A_1 for the "turned-off" transistor collector for pin 4 and pin 5. Record the current.

3.2.4 Specified current should be $\bar{>}$ 5 μ amps.

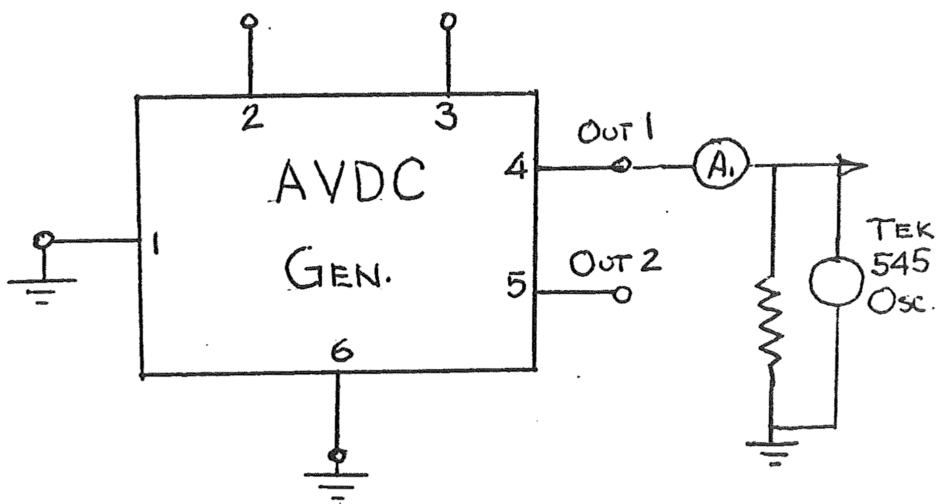


Fig. 3

3.2.5 Measurement Procedure. "0" Level. Connect a DC VTVM capable of reading 100 mv between terminals T_1 and T_2 as shown in Figure 4. Adjust R_4 for 100 mv on V_1 and set R_2 at midscale. Connect the AVDC generator as shown in Figure 4 and adjust R_5 for 50% duty cycle on the oscilloscope waveform. Connect the AC current probe between pin 4 and the 10Ω load. Record the current and voltage of the saturated transistor. Repeat for pin 5.

3.2.6 Specified output should be 50 ma maximum at 0.5 V maximum.

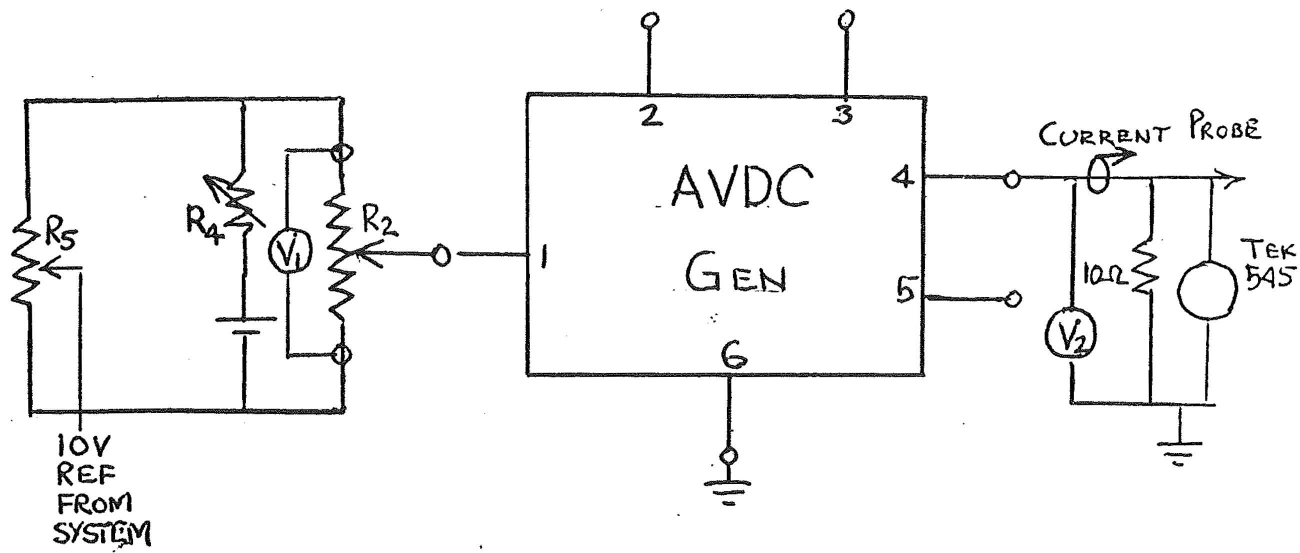


Fig. 4

3.3 Input Signal

3.3.1 Required Equipment: Tektronix 545, DC DVM, .1% Leeds & Northrup Potentiometer, DC VTVM.

3.3.2 Connect a DC VTVM capable of reading 100 mv between terminals T_1 and T_2 as shown in Figure 5. Adjust R_4 for 100 mv on V_1 and set R_2 at 10.00. Adjust R_5 for 3% duty cycle on the oscilloscope waveform. Set R_2 at 5.00 and connect a DC DVM to pin 1 of the AVDC generator. Record the voltage reading.

3.3.3 Specified voltage should be 10 $\pm$ .05 V.

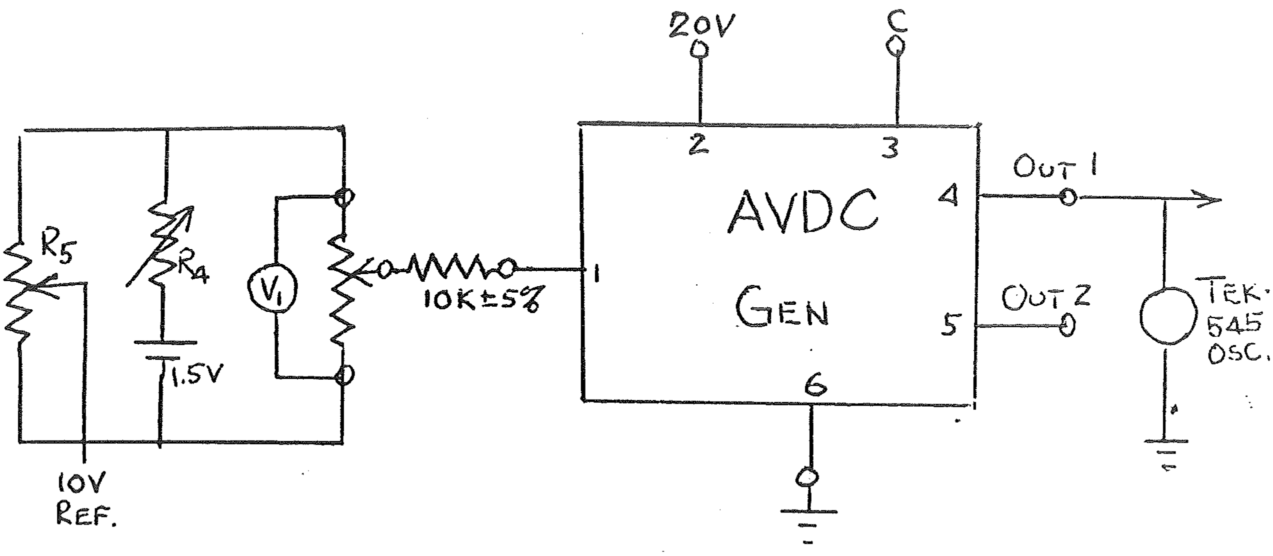


Fig. 5

3.4 Circuit Sensitivity

3.4.1 Required Equipment: Tektronix 545 oscilloscope, .1% Leeds & Northrup Potentiometer, DC VTVM.

3.4.2 Connect a DC VTVM capable of reading 100 mv between terminals T_1 and T_2 as shown in Figure 5. Adjust R_4 for 100 mw on V_1 and set R_2 at 10.00. Adjust R_5 for 3% duty cycle on the oscilloscope waveform. Connect the time delay base of the Tektronix 545 oscilloscope to pin 4 and use the output of the delay to trigger the oscilloscope. Vary R_2 to 0 setting, then adjust the oscilloscope delay potentiometer to locate the vertical midpoint of the falling edge of the waveform trace to the center of the oscilloscope graticule. Read the record the setting on the oscilloscope time delay dial. Readjust the delay potentiometer on the falling edge of the full period trace and again record the delay dial setting. Repeat for 50% duty cycle or R_2 = 5.0 on dial.

3.4.3 Sensitivity should be nominally 1% in output D.C. change for 1 millivolt signal input change.

$$\text{Sensitivity} = \frac{\text{50\% Reading - 0\% Reading}}{\text{100\% Reading}} \times \frac{1}{50} \times 100$$

$$= \frac{\text{\% D.C. } \Delta}{\text{mv}}$$

3.5 Circuit Stability

3.5.1 Required Equipment: Tektronix 545 oscilloscope, .1% Leeds & Northrup Potentiometer, DC VTVM.

3.5.2 Connect a DC VTVM capable of reading 100 mv between terminals T_1 and T_2 as shown in Figure 5. Adjust R_4 for 100 mv on V_1 and set R_2 at 10.00. Adjust R_5 for 3% duty cycle on the oscilloscope trace. Set R_2 at 5.0 on the dial and connect the DC VTVM to pin 2 of the AVDC generator capable of reading 30 V full scale. Read the R_2 dial, then vary V_{cc} plus and minus 1 volt, readjusting R_2 each time to maintain 50% duty cycle and reading the R_2 dial for these two extremes.

3.5.3 Maximum specified variation should be $\pm$ 0.25 volt for all temperature and voltage variations.

3.6 Output Linearity

3.6.1 Required Equipment: Tektronix 545 oscilloscope, .1% Leeds & Northrup Potentiometer, DC VTVM.

3.6.2 Connect a DC VTVM capable of reading 100 mv between terminals T_1 and T_2 as shown in Figure 5. Adjust R_4 for 100 mv on V_1 and set R_2 at 10.00. Adjust R_5 for 3% duty cycle on the oscilloscope trace. Vary R_2 from 0 to 10.00 in one increment steps, then adjust the oscilloscope delay potentiometer to locate the vertical midpoint of the falling edge of the waveform trace to the center of the oscilloscope graticule. Read and record the potentiometer dial setting on the oscilloscope time delay dial.

3.6.3 The maximum specified departure from linearity will be 2.5 percentage points.

3.7 Output Time Symmetry

3.7.1 Required Equipment: Tektronix 545 oscilloscope, .1% Leeds & Northrup Potentiometer, DC VTVM.

3.7.2 Connect a DC VTVM capable of reading 100 mv between terminals T_1 and T_2 as shown in Figure 5. Adjust R_4 for 100 mv on V_1 and set R_2 at 10.00. Adjust R_5 for 3% duty cycle on the oscilloscope trace. Adjust R_2 for 5.0 on the dial.

3.7.3 Read the 10% rise and fall time on the oscilloscope trace by adjusting the oscilloscope delay potentiometer to locate the vertical midpoint of the falling edge of the waveform trace to the center of the oscilloscope graticule. Read and record the setting on the oscilloscope time delay dial. Make readings at both pins 4 and 5 reading the rise and fall times of each output.

3.7.4 The specified on time symmetry shall be that the "on" time of one output shall be .5% of the "on" time of the other output. Also, the half period time shall be $\pm$ .25% of the absolute value of the half period time.

3.8 Rise and fall time.

3.8.1 Required Equipment: Tektronix 545 oscilloscope, .1% Leeds & Northrup Potentiometer, DC VTVM.

3.8.2 Connect a DC VTVM capable of reading 100 mv between terminals T_1 and T_2 as shown in Figure 5. Adjust R_4 for 100 mv on V_1 and set R_2 at 10.00. Adjust R_5 for 3% duty cycle on the oscilloscope trace. Set R_2 at 5.0 on the dial and read the rise and fall time of the output waveform at pin #4 and pin #5.

3.8.3 Specified rise and fall time should be $\leq$ 0.5 μsec from zero to maximum output and vice versa.

Table I Comparison of Analog and Digital Systems

Factor	Digital Approach	Analog Approach
ACCURACY:		
Linearity	± 0.3% ladder matching ± 0.4% P.S. regulation	± 0.5%
Sensitivity	± 0.3%	± 0.3%
Power Dissipation	2.0 watts	1.3 watts
HIGH FREQUENCY SPIKES:		
Ramp	Faster switching	None required
Amplifier	Separation power supply	None required
Signal	Lock-out, etc.	Lock-out, etc.
Frequency Shaping	Limited by noise rejection	Open loop rolloff
Complexity	Analog system requires 60% fewer components	
Number of Chips	2 processes	1 process

Table II Comparative Parts Count

Description	Capacitor	Transistors	Diodes	Resistors		TOTAL
Blocks associated with DIGITAL APPROACH ONLY						
Time Base	2	2		4		
Binary Counter	18	18	98	72		
Ladder		16		57		
Ladder Supplies	—	6	—	12		
	20	42	98	145	=	305
ANALOG and DIGITAL Blocks						
Difference Amplifier	3	12	4	22		
Reference Supply	2	4	5	7		
Comparator		4	3	7		
Output Logic	—	4	6	6		
	5	24	18	42	=	89
ANALOG ONLY Blocks						
Triangle Gen.	2	19	7	28		
2.5 kc Binary	2	2	12	8		
	4	21	19	36	=	80
DIGITAL TOTAL	25	66	116	187	=	394
ANALOG TOTAL	9	45	37	78	=	169
Difference	16	21	79	109	=	225

57% Reduction in Parts Count

Table III Comparative Parts Count, Including Final Design

	Capacitors	Transistors	Diodes	Resistors	TOTAL
1. Digital System, 1st Design	25	66	116	187	394
2. Analog System, 1st Design	9	45	37	78	169
3. Analog System, Final Design	10	33	32	71	146

Table IV Power Requirements

DIGITAL ONLY		
Time Base	15 ma	
Binary Counter	20	new design
Ladder	0	old design = 60
Ladder Supplies	20	
	55	
ANALOG and DIGITAL		
Difference Amplifier	15	
Reference Supply	25	
Comparator	2	
Output Logic	6	
	48	
ANALOG ONLY		
Triangle Generator	15	
2.5 kc Binary	2	
	17	
DIGITAL TOTAL	103	= 2.06 watts
ANALOG TOTAL	65	= 1.30 watts
Difference	38	= 37% reduction

Table V   Comparative Power Requirements, Including Final Design

	POWER, WATTS				
	Voltage Reference	Error Amplifier	Ramp Generator	Output Stage	TOTAL
1. Digital System, 1st Design	0.50	0.30	1.10	0.16	2.06
2. Analog System, 1st Design	0.50	0.30	0.30	0.20	1.30
3. Analog System, Final Design	0.18	0.30	0.17	0.23	0.88

Table VI Pertinent Characteristics of Subsystem Components

Component	Major D.C. Characteristic(s)	Temperature Coefficient	Range of values, -10°C to +75°C
Transistor, single unit	V_{BE} at constant I_C, V_{CE}: $\simeq +0.7V$ $\beta: \geqslant 50$	2.3 mV/°C	+ 0.62 to + 0.82 $\beta: \geqslant 30$
Transistor, differential pair	$\Delta V_{BE}(V_{BE_1}-V_{BE_2})$ at constant I_C, V_C: $\leqslant 0.04V$	$\leqslant$ 20 µV/°C	$\Delta V_{BE}(25°C) \pm 1.0$ mV
Resistor, diffused, single unit	$R := R_{design} \pm 10\%$	+ 2000 ppm/°C	$0.95\ R_{25°C}$ to $1.11\ R_{25°C}$ (200 Ω/□) $0.92\ R_{25°C}$ to $1.12\ R_{25°C}$ (250 Ω/□)
Resistor pair, diffused	$\frac{R_1}{R_2} := \left(\frac{R_1}{R_2}\right)_{design} \pm 5\%$	$\leqslant$ 20 ppm/°C	$\left(\frac{R_1}{R_2}\right)_{25°C} \pm .1\%$
Resistor, tantalum nitride, single unit	$R := R_{design} \pm 5\%$	-100 ppm/°C	$R_{25°C} \pm 0.5\%$
Resistor pair, tantalum nitride	$\frac{R_1}{R_2} := \left(\frac{R_1}{R_2}\right)_{design} \pm 2\%$	$\leqslant$ 2 ppm/°C	$\left(\frac{R_1}{R_2}\right)_{25°C} \pm .01\%$
Capacitor, tantalum film	$C := C_{design} \pm 5\%$	200 ppm/°C	$C_{25°C} \pm 1\%$
Diode Zener reference	$V_z := 6.4V \pm 0.4V$	$\leqslant$ 20 ppm/°C (including series forward diode)	$(V_z)_{25°C} \pm 6$ mV (including series forward diode)

Table VII Performance Characteristics of Subcircuits

Subcircuit	Signal or Characteristic Designation	Nominal Value and Tolerance, 25°C	Design Value and Tolerance, 25°C	Design Limiting Values -10°C to +75°C	Fractional Contribution To Specification Limit of Subsystem	
					Specification Designation	Fractional Contribution
1. Error Amplifier	V_i-Input Voltage	$10.000V \pm 0.010V$ center value*		$(V_i)_{25°} \pm 0.02V$ center value*	No. 6-<u>Input Signal</u> and No.12-<u>Circuit Stability</u>	0.8
	V_E	$5.00\ V \pm 0.25\ V$ center value*		$(V_E)_{25°} \pm 0.05V$	No.12	0.05
	A_E	$40\ {+15 \atop -3}$	45 ± 5	$(A_E)_{25°} \pm 1$	No. 7-<u>Circuit Sensitivity</u>	0.95
2. Voltage Reference	V_R-Reference Voltage	10V	$10V \pm 0.15V$ initially adjusted for $10.000\ V \pm 0.010V\ V_i$ center value	$(V_R)_{25°} \pm 0.010V$	No. 6 No.12	1.0, by init. adj. 0.5
3. Triangle Generator	V_L-Level Voltage	$V_{L(high)} = 7V$ $V_{L(low)} = 3V$	$V_{L(high)} = 7V \pm 0.35V$ $V_{L(low)} = 3V \pm 0.15V$	$(V_L)_{25°} \pm 0.1V$	No.12 No. 1-<u>Rep.Rate</u>	0.1 0.25
	$\dot{V}_{TR}$-Triangle Voltage Slope	$\dot{V}_{TR} = 4V/100\ \mu s$	$4V \pm 0.2V/100\ \mu s$	$(\dot{V}_{TR})_{25°} \pm \frac{0.06V}{(100\mu s)}$	No. 1	0.2
	$\ddot{V}_{TR}$-Triangle Voltage Change of Slope	$\ddot{V}_{TR} = 0$	$0 \pm 0.1V/(100\ \mu s)^2$	$0 \pm 0.1V/(100\ \mu s)^2$	No. 8-<u>Output Linearity</u>	0.2
4. Comparator & Output Circuit	V_{01}, V_{02} - Output Voltage	$V_o \leqslant 0.4V$ at $I_{load} = -50$ mA	$V_o \leqslant 0.4\ V_c$ at $I_{load} = -50$ mA	$V_o \leqslant 0.5V$	No. 2-<u>Output Level</u>	1.0

* Center value = value for 50% duty cycle output

TABLE VIII

AVDC TEST RESULTS

	Parameter	Specification	Units	Temp.	#1	#2	#3	#4	#5
	Pin Connect				#4 #5	#4 #5	#4 #5	#4 #5	#4 #5
1	Period	400 ± 40	μsec	-10°C +75°C	395 430	425 435	440 455	350 420	415 440
2	Output Sw. Saturation "0" Level	≤ 0.5 @ 50 ma	volts	-10°C +75°C	0.20 0.25 0.35 0.40	0.30 0.35 0.35 0.40	0.40 0.35 0.50 0.45	1.00 1.00 1.45 1.50	0.30 0.50 0.45 0.50
3	Output Sw. Leakage "1" Level	5 @ 20 V	μamps	-10°C +75°C	<1 <1 4 3.7	<1 <1 8 10	<1 <1 5 4	10 9 20 15	2 1 5 4
4	Input Signal	10 ± .05	volts	-10°C +75°C	10.500 9.950	10.500 10.400	10.240 10.080	10.800 10.450	9.750 9.520
5	Sensitivity	1.0 or 3% to 97%	%/mv	-10°C +75°C	0.90 0.95	0.94 0.91	1.2 1.0	1.5 1.0	0.95 0.91
6	Stability	± 25	mv	-10°C +75°C	+9.0 -2.2 +8.0 -1.6	+5.3 -3.1 +7.5 -8.3	+6.7 -10.0 +3.1 -13.6	+6.0 -15.0 +2.7 -18.0	2.4 6.0 2.0 9.0
7	Linearity	± 2.5	%FS	-10°C +75°C	±1.25 ±1.15	±2.00 ±2.00	±1.25 ±1.15	±1.75 ±2.00	±1.25 ±1.15
8	Symmetry "ON" Time	≤ 0.5	%	-10°C +75°C	0.0 0.0	.4 .4	.4 .4	0.3 0.3	0.4 0.0

TABLE VIII

AVDC TEST RESULTS

(Continued)

	Parameter	Specification	Units	Temp.	#1	#2	#3	#4	#5
	Pin Connect				#4 #5	#4 #5	#4 #5	#4 #5	#4 #5
9	Symmetry Half Period	± .25	%	-10°C +75°C	±.50	±2.5	±2.0	±.50	±.25
10	Rise Time	0.5	μsec	-10°C +75°C	0.3 0.4	0.2 0.1	0.3 0.1	0.3 0.2	0.4 0.1
11	Fall Time	0.5	μsec	-10°C 75°C	0.2 0.3	0.3 0.2	0.4 0.2	0.4 0.1	0.2 0.1
	Item Out Of Spec				4, 9	3, 4, 9	1, 4, 5	2,3,4,5,9	4

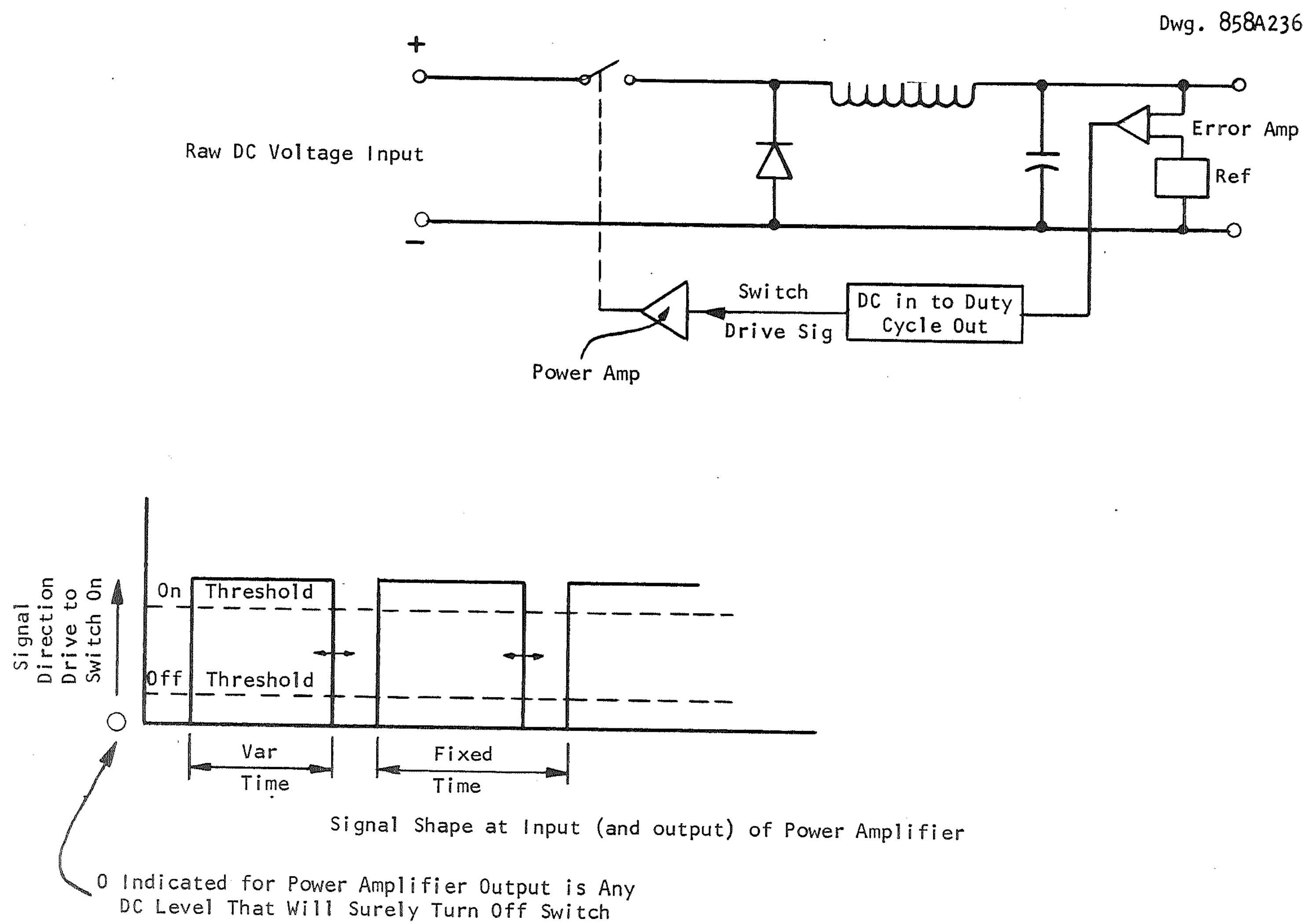


Fig. 1—Typical down regulator

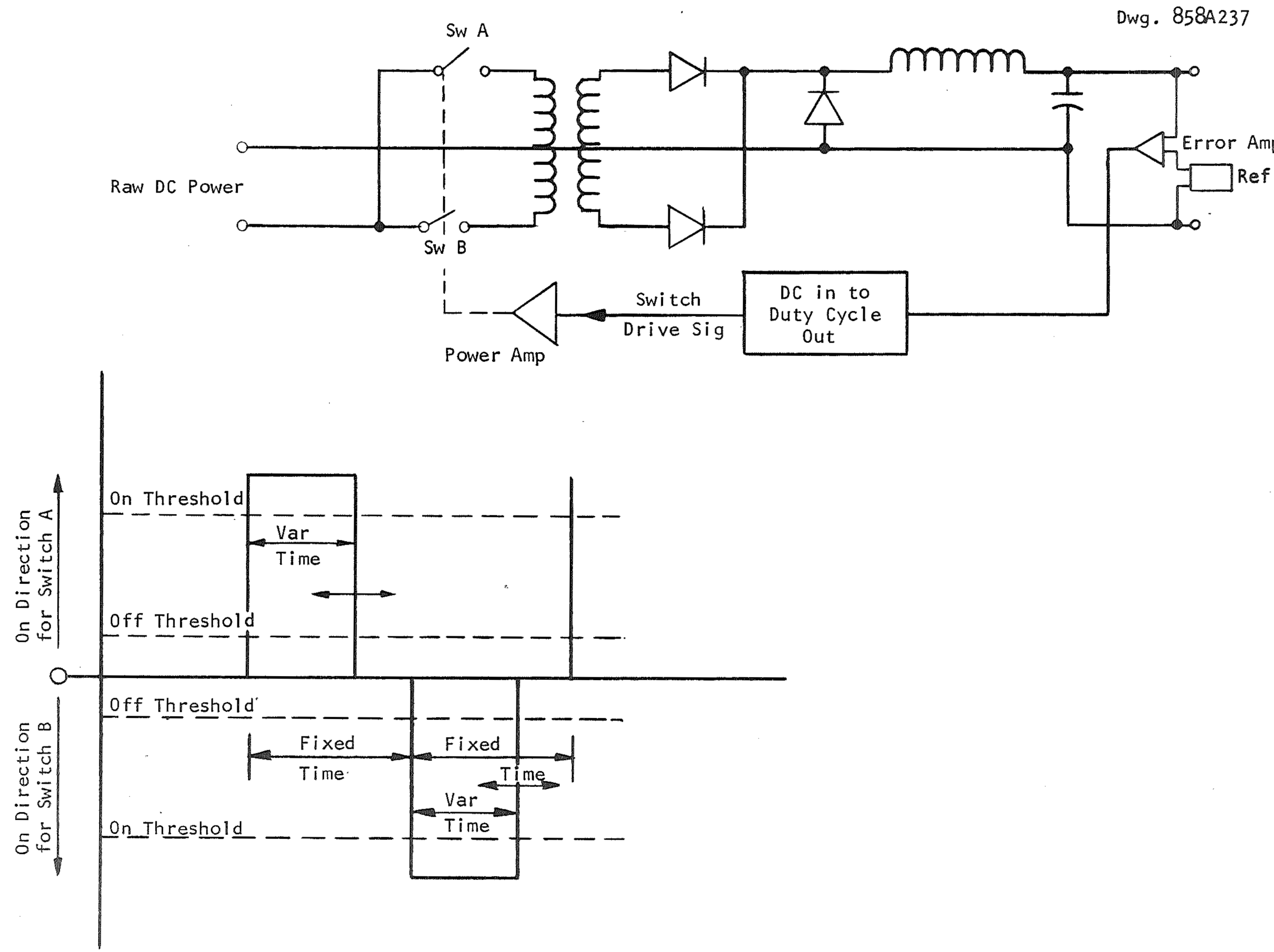


Fig. 2—Typical booster regulator

Dwg. 858A238

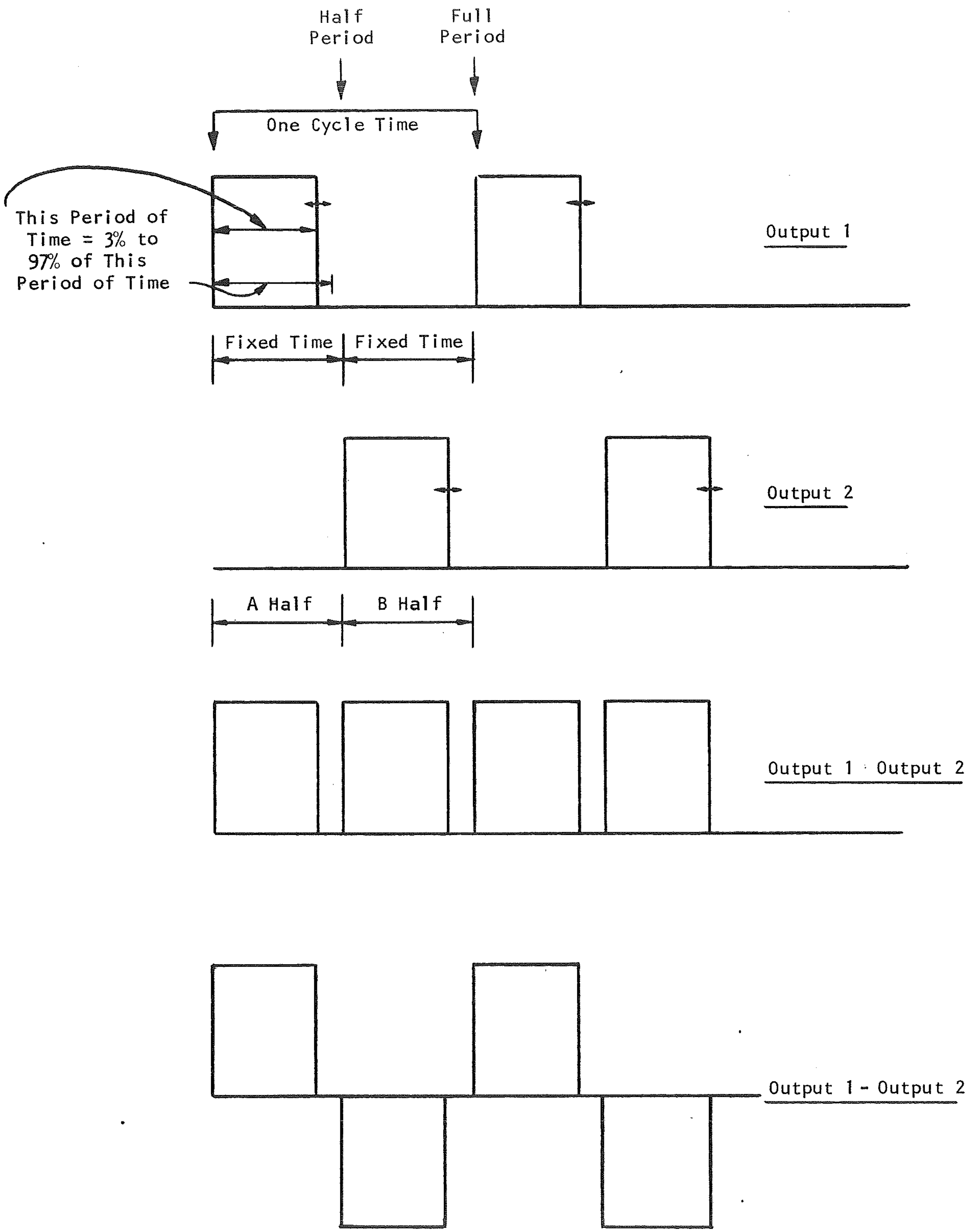


Fig. 3—Regulator output mixing

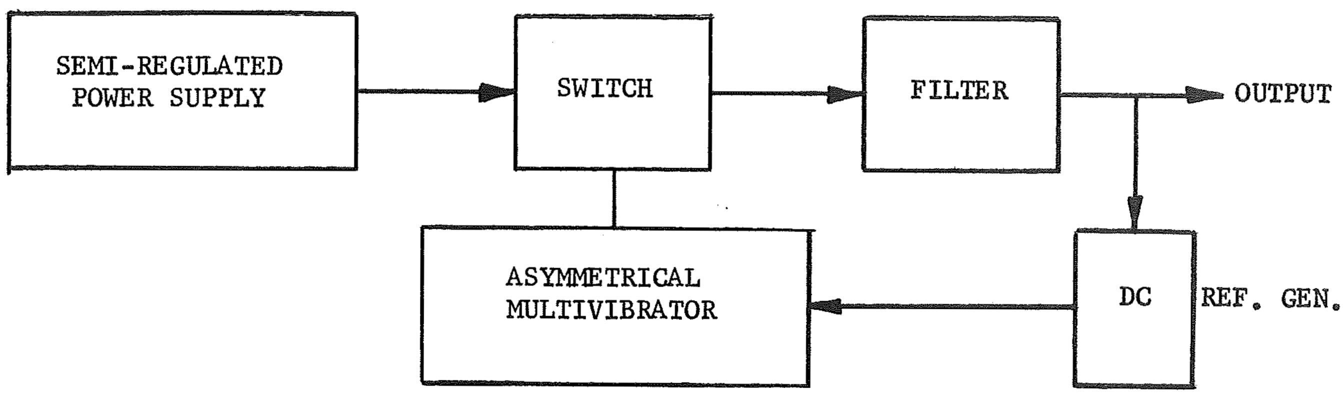


Fig. 4 Variable Duty Cycle Regulator

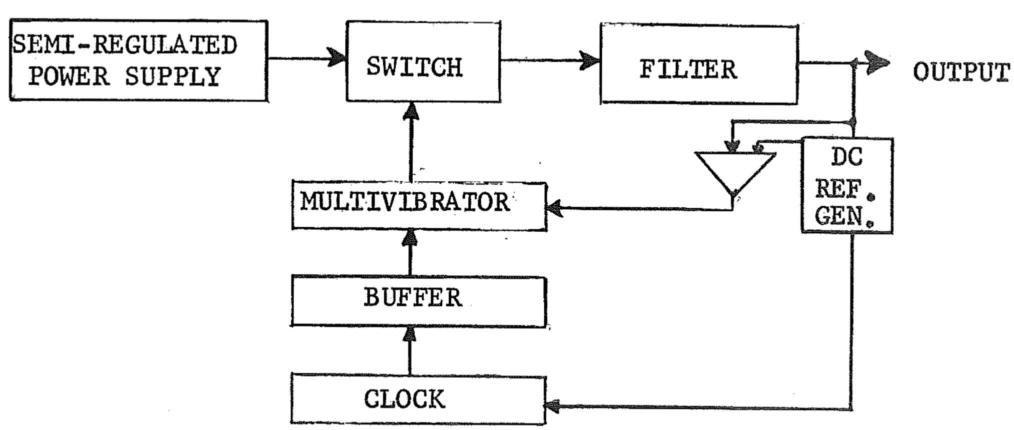


Fig. 5 Clocked Multivibrator

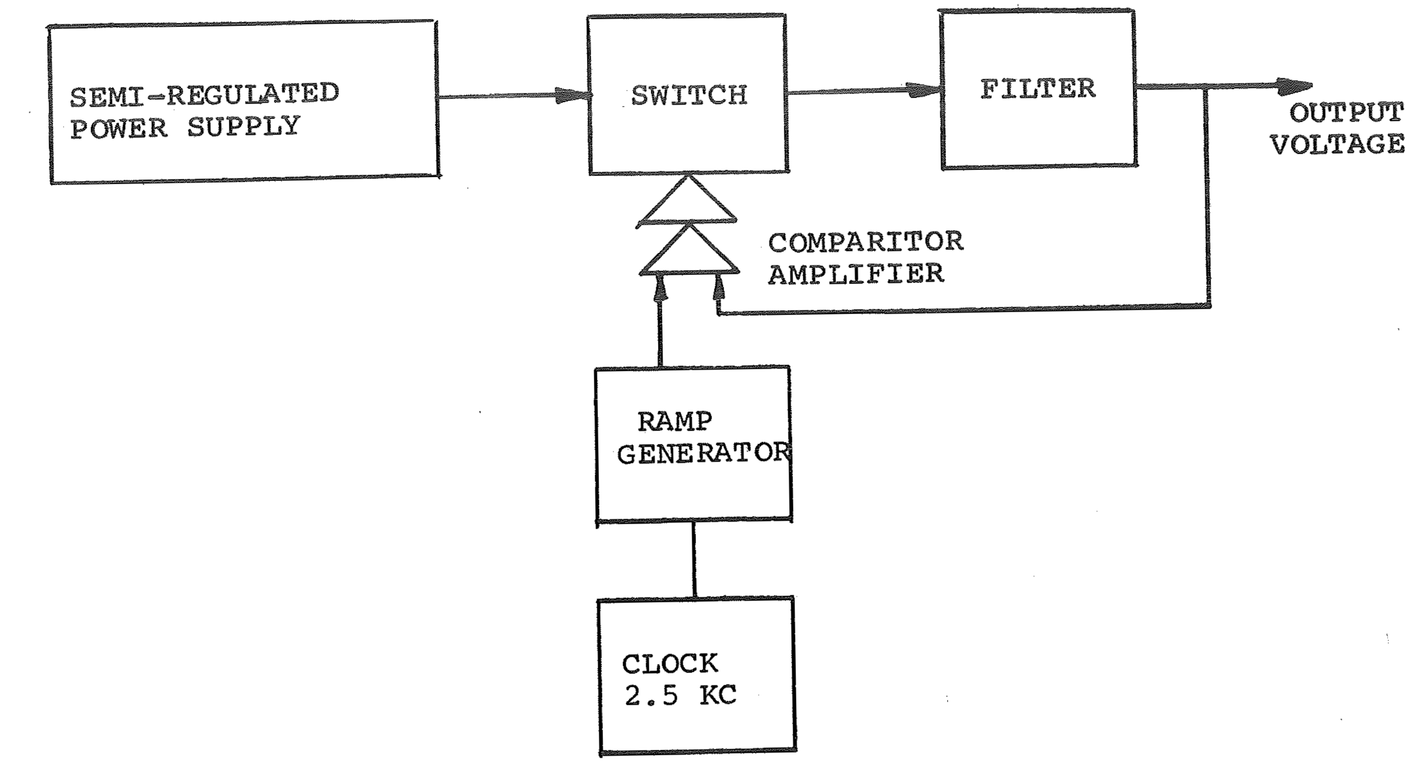


Fig. 6 Analog Ramp Generator

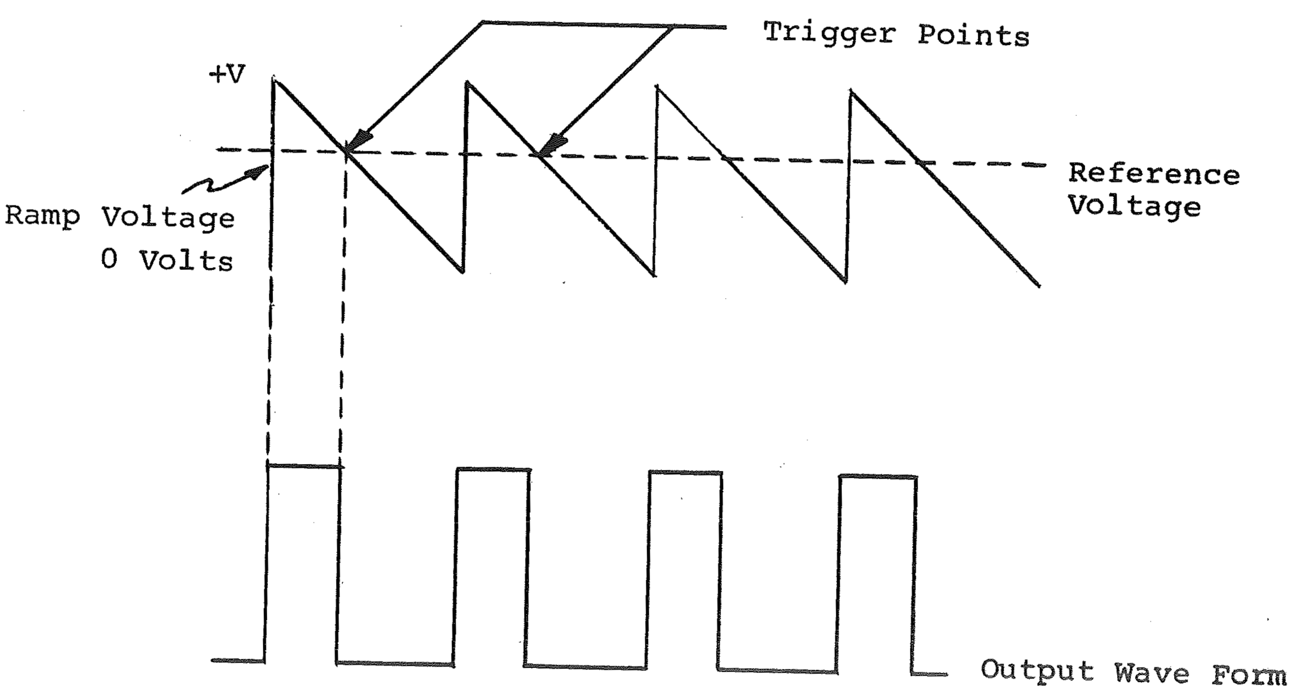


Fig. 7 Waveforms for Analog Ramp Generator

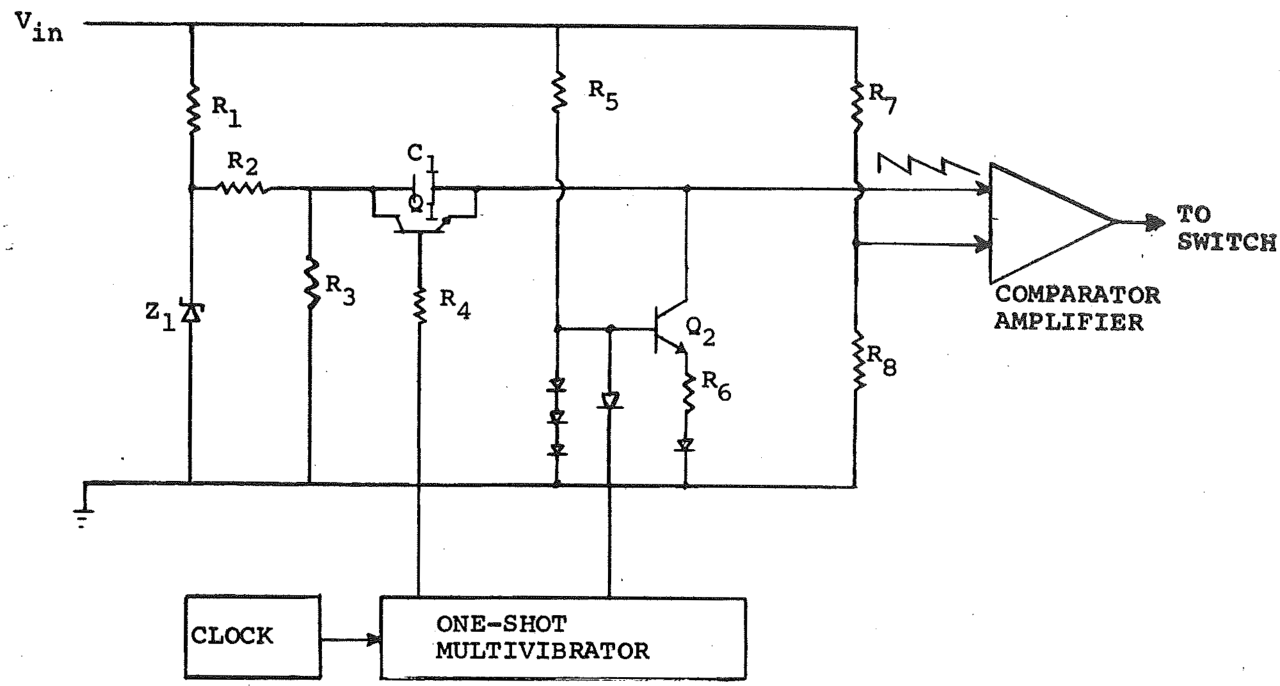


Fig. 8 Ramp Generator Control Circuit

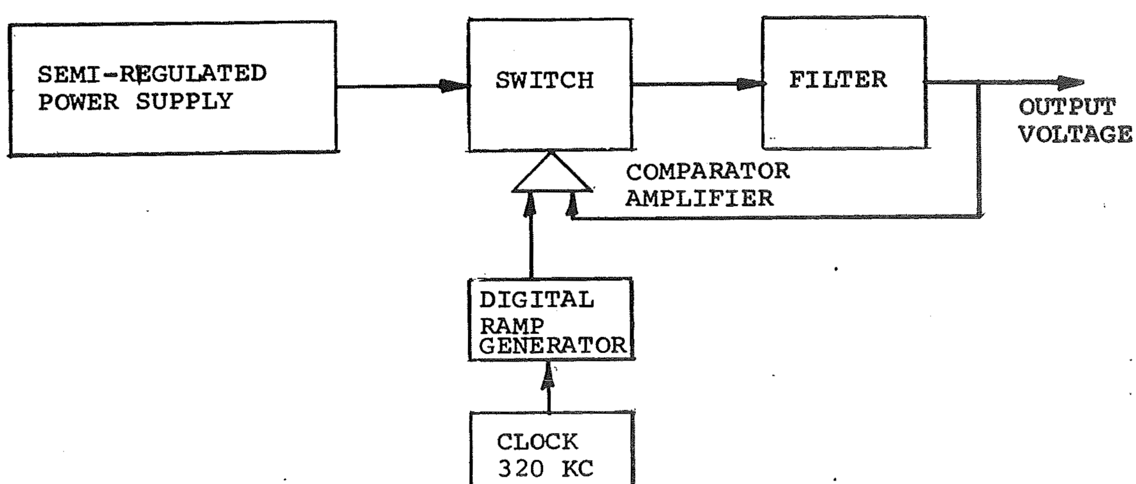


Fig. 9 - Block Diagram for Digital Ramp Generator

Dwg. 858A239

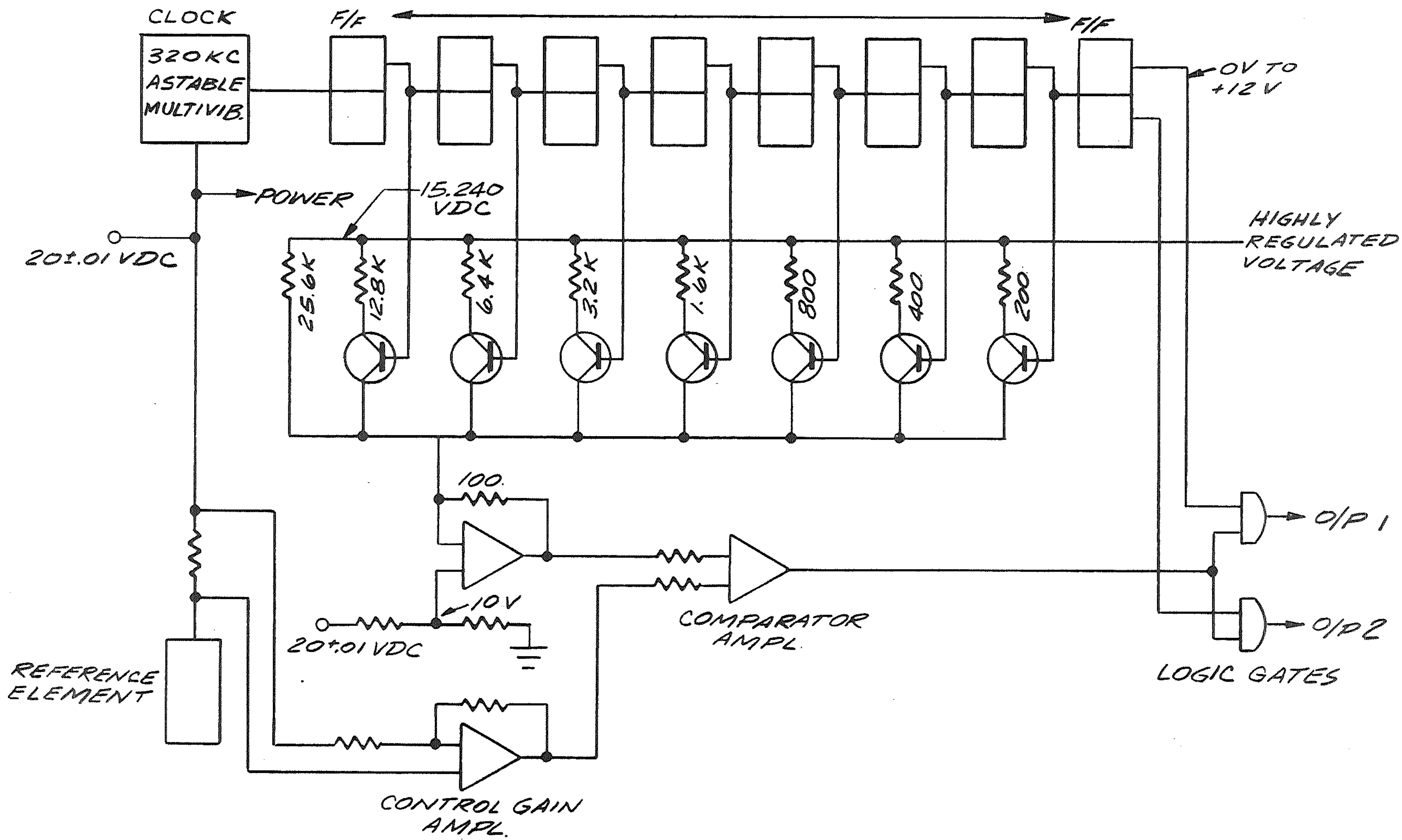


Fig. 10—Digital block diagram

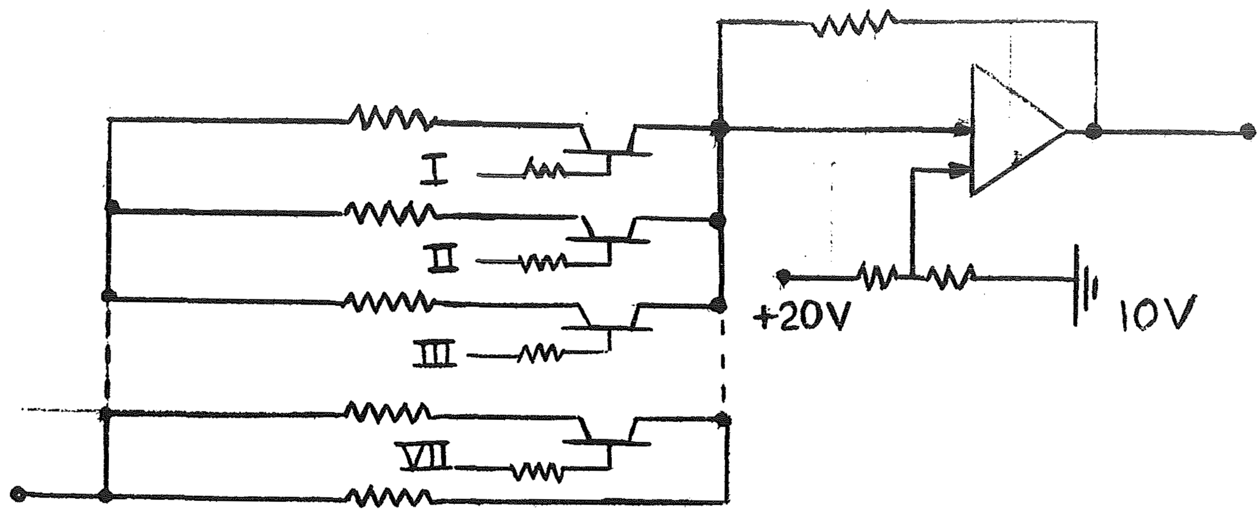


Fig. 11 Ramp Generator (Simplified Form)

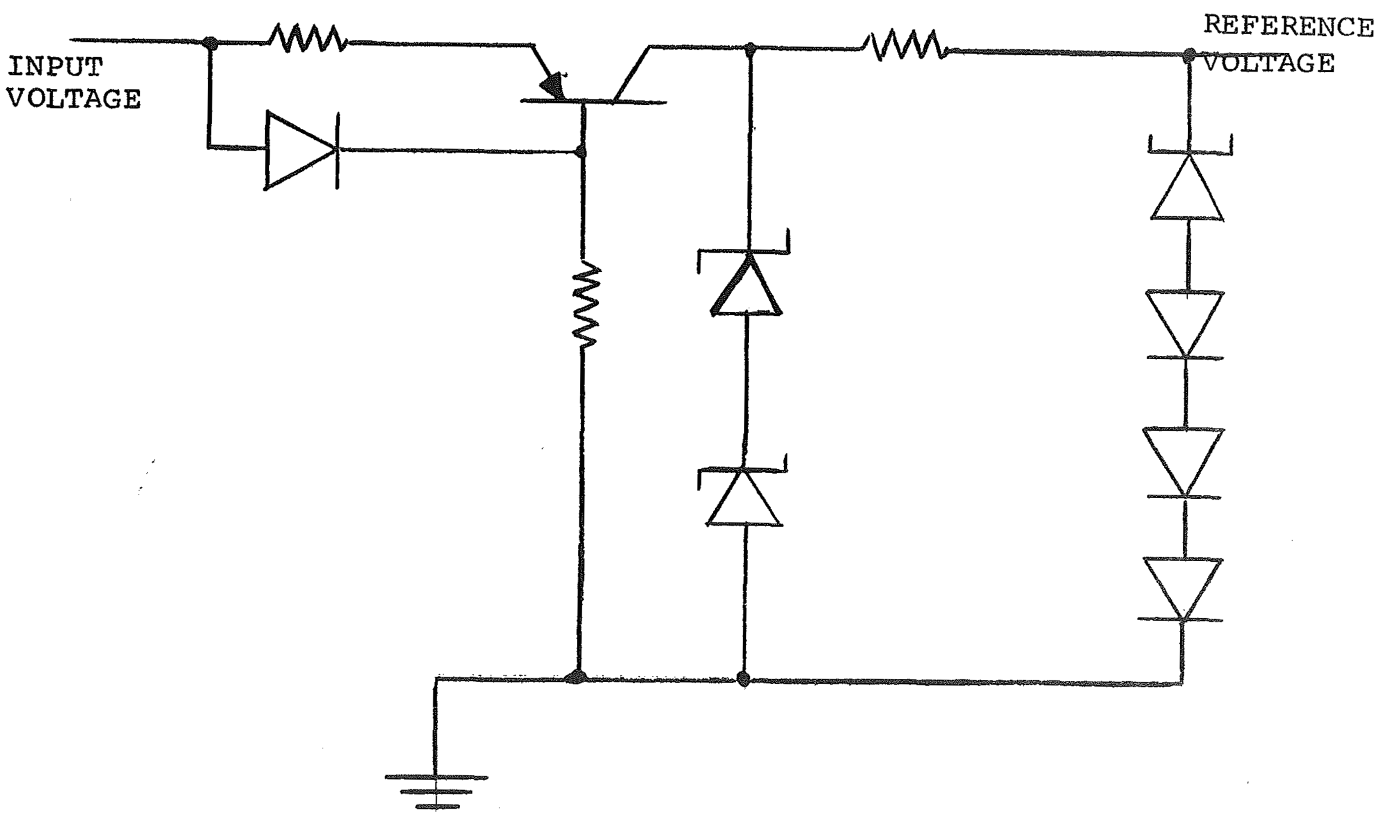


Fig. 12 Precision Reference Source

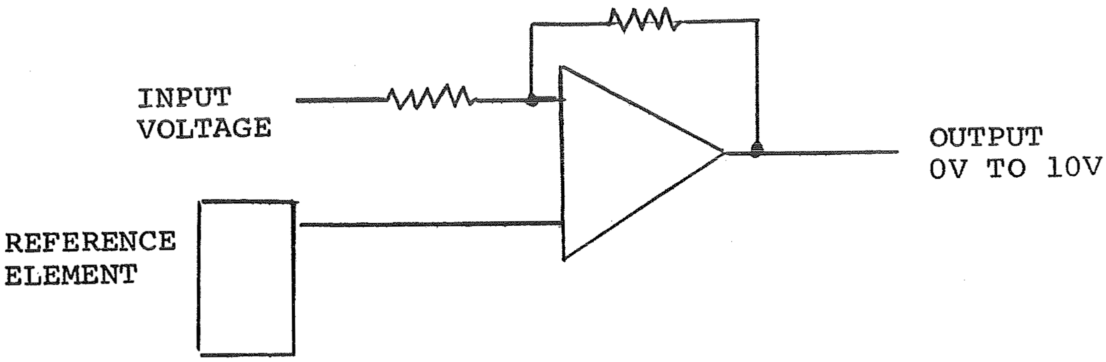


Fig. 13 Error Amplifier Block Diagram

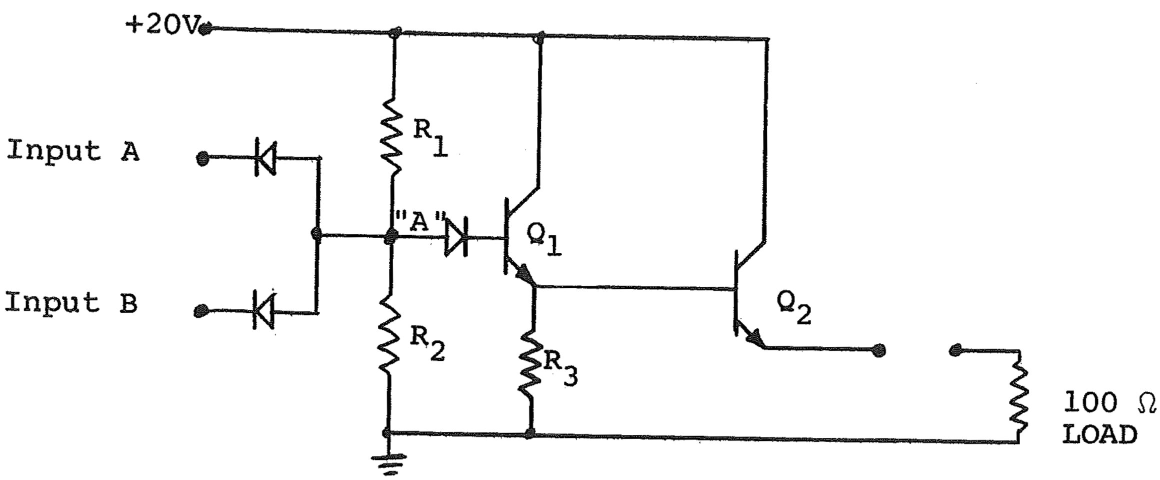


Fig. 14 Output Circuit (Simplified Form)

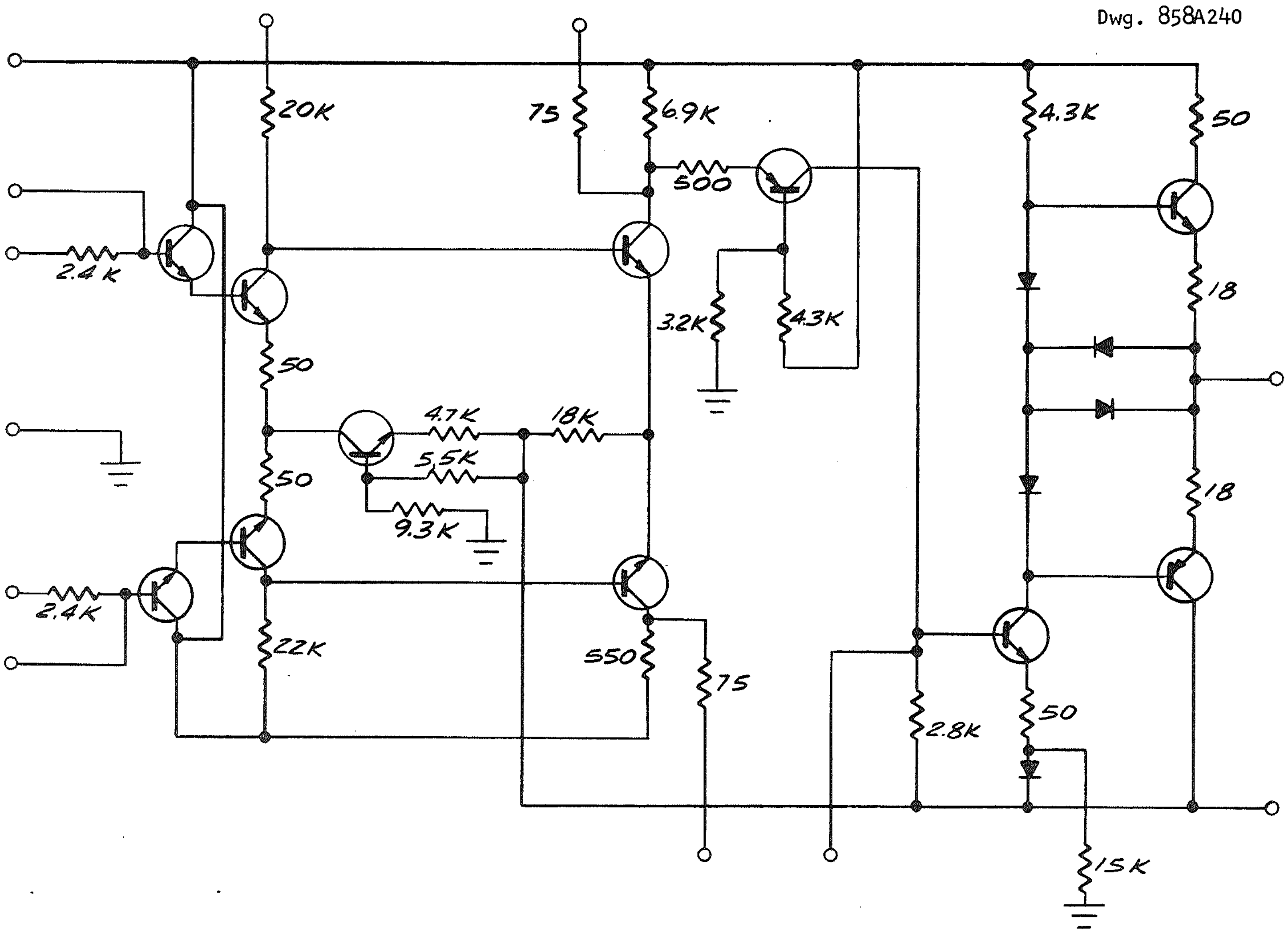
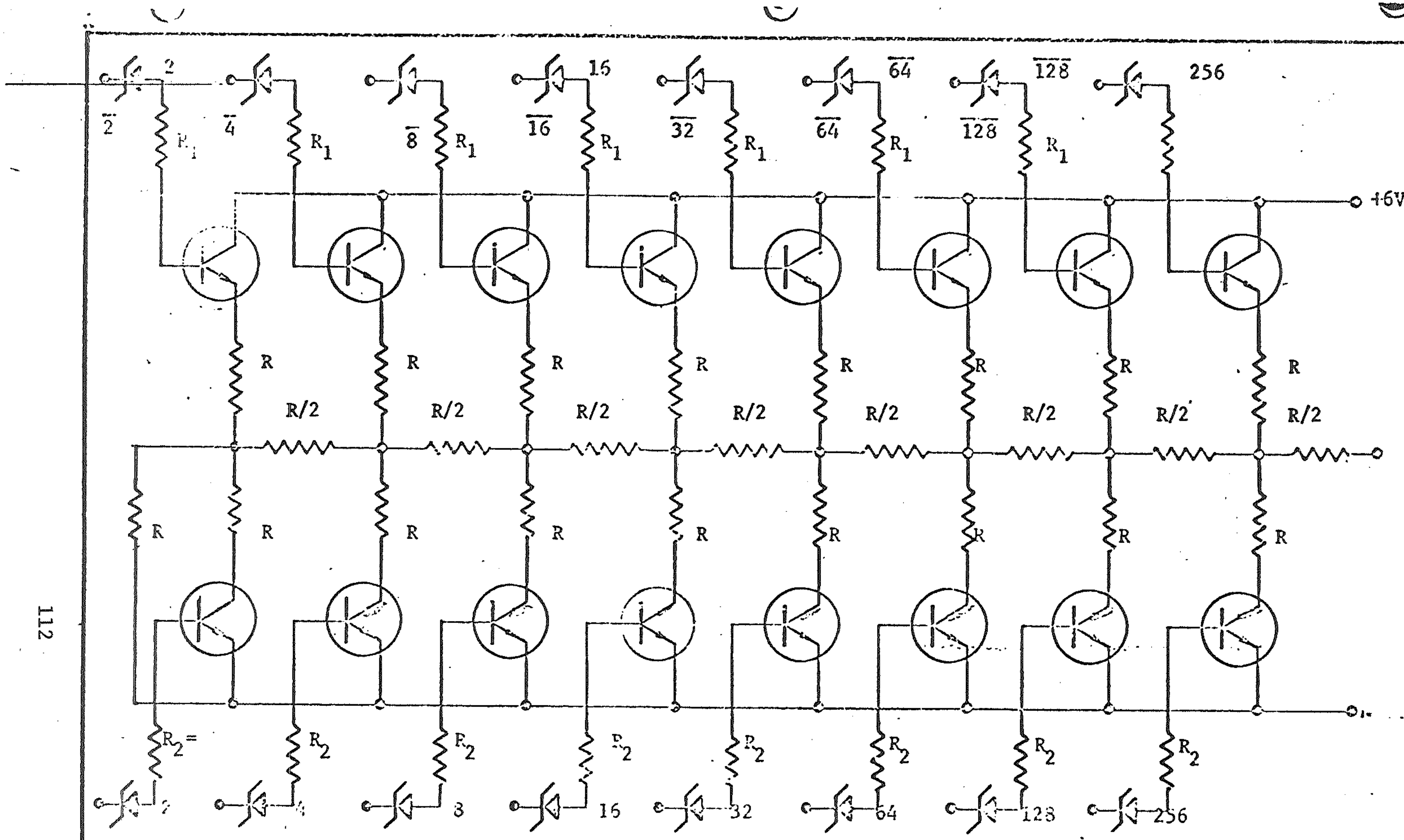


Fig. 15—Operational amplifier



R = 5K
V_Z = 8V
R_1 = 1K
R_2 = 8K

Fig. 16 LADDER NETWORK

Dwg. 852A934

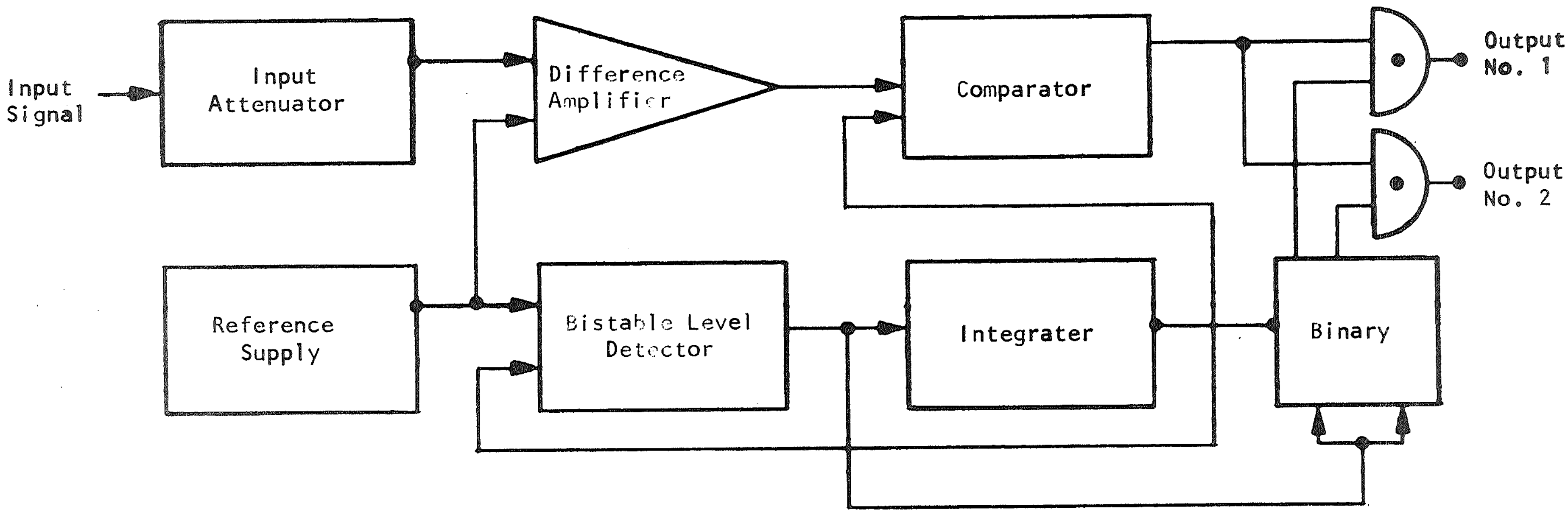


Fig. 17 —Analog system block diagram

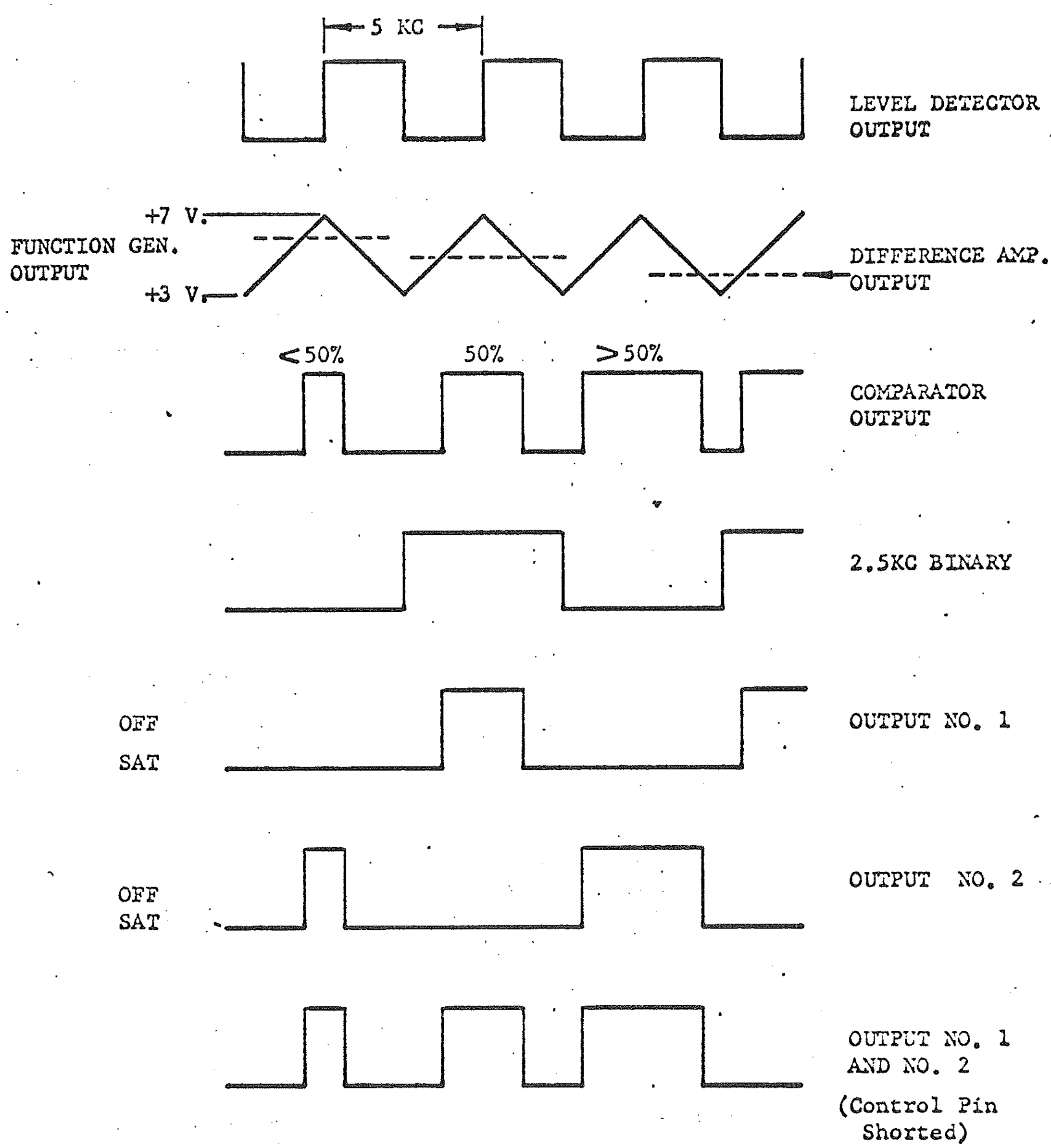


Fig. 18 TIMING AND LOGIC DIAGRAM

Dwg. 858A241

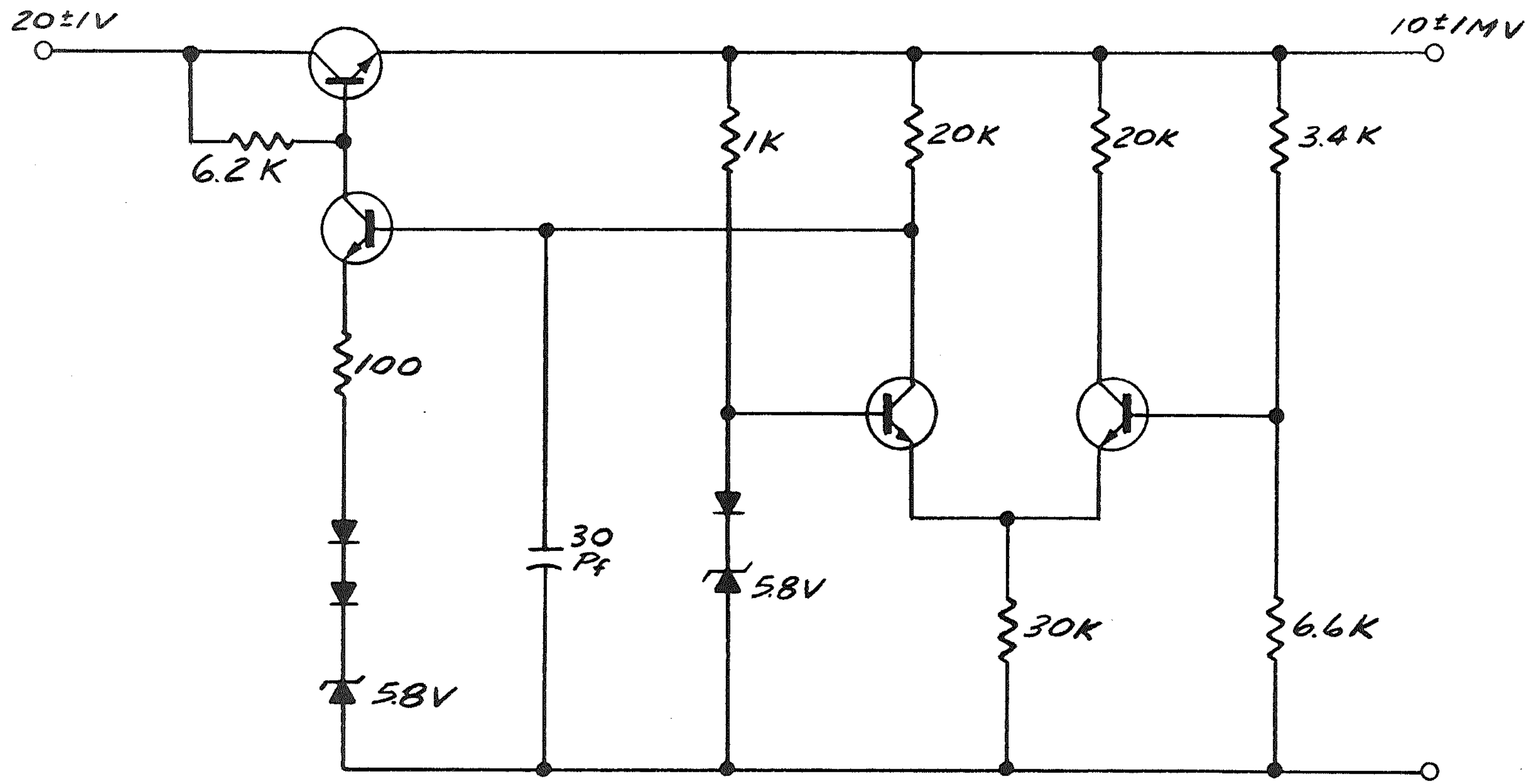


Fig. 19—Voltage reference, first analog design

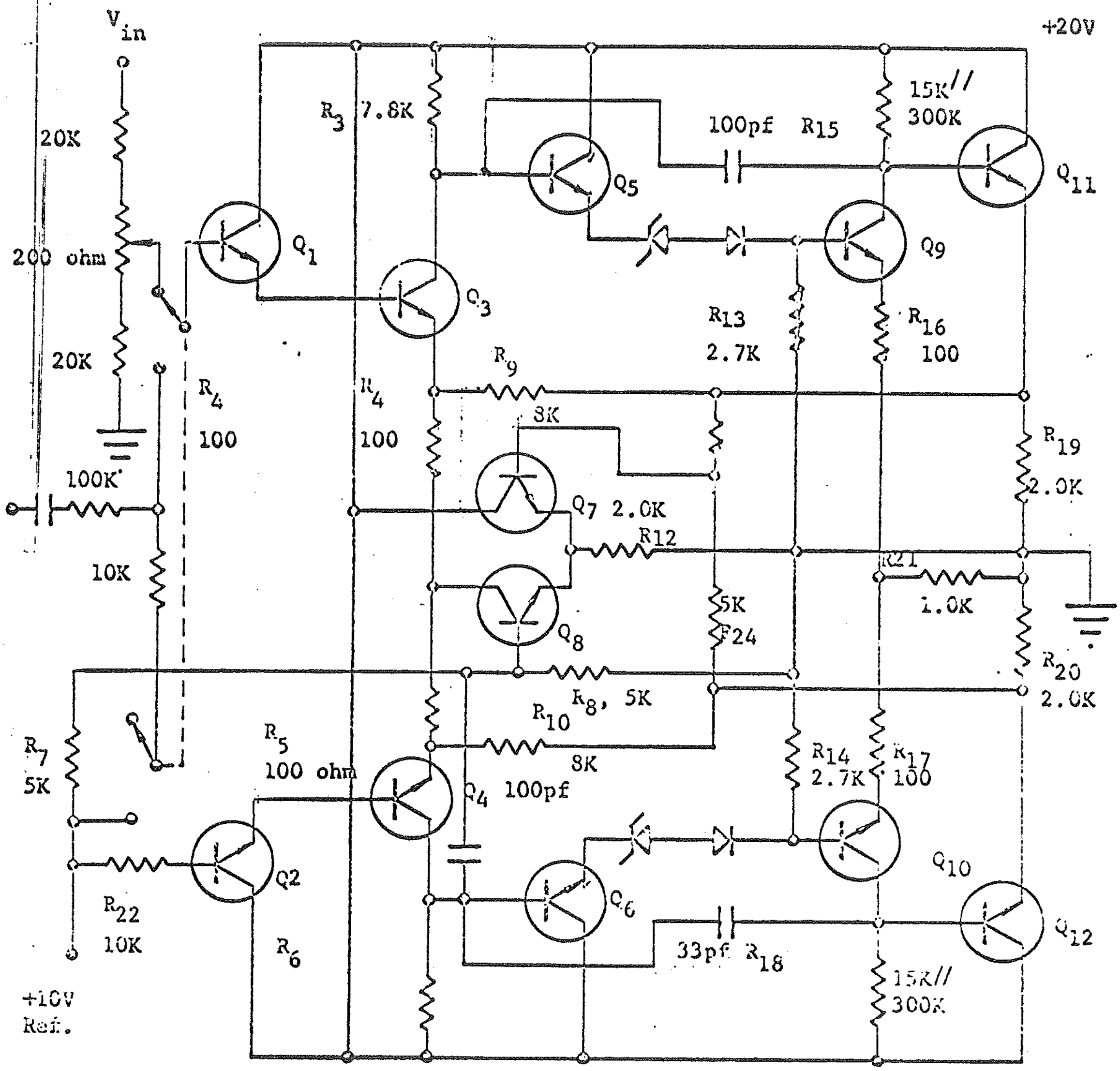


Fig. 20 Error Amplifier, First Analog Design

Dwg. 721B465

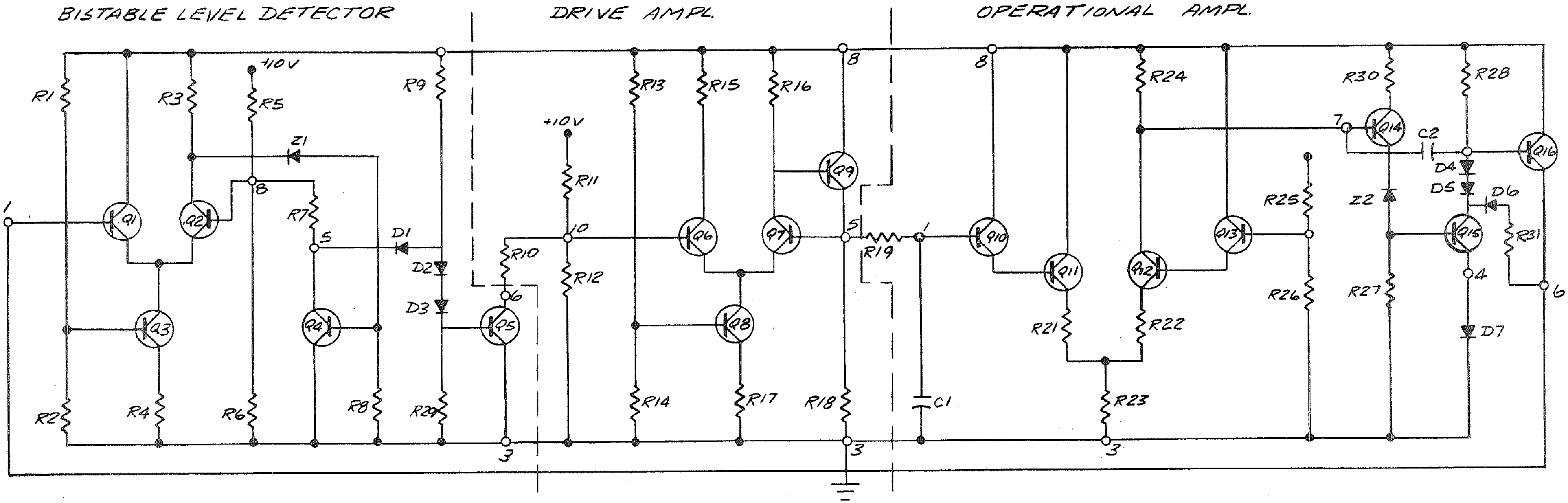


Fig. 21—Triangle generator, first analog design

Dwg. 858A242

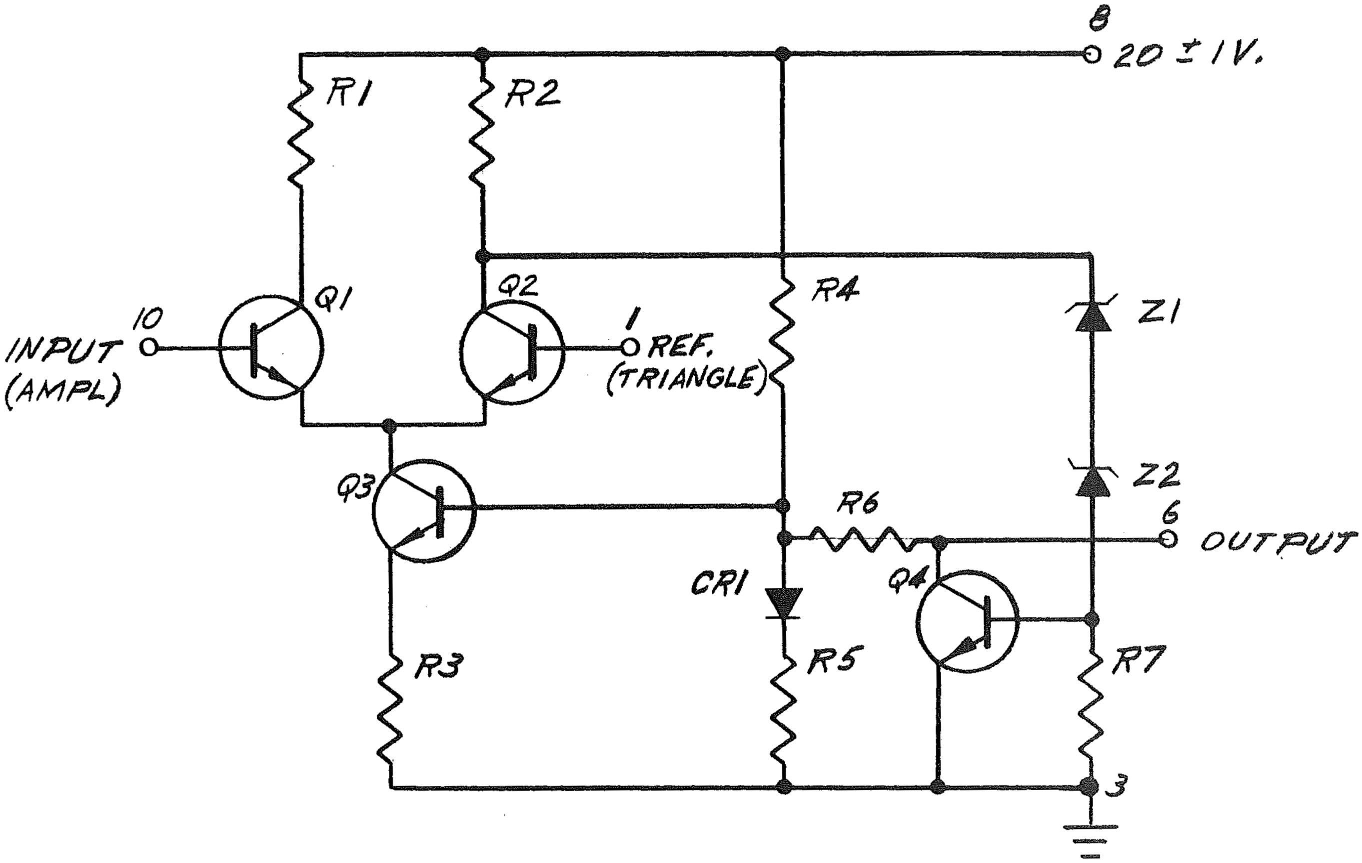


Fig. 22—Output circuits, first analog design

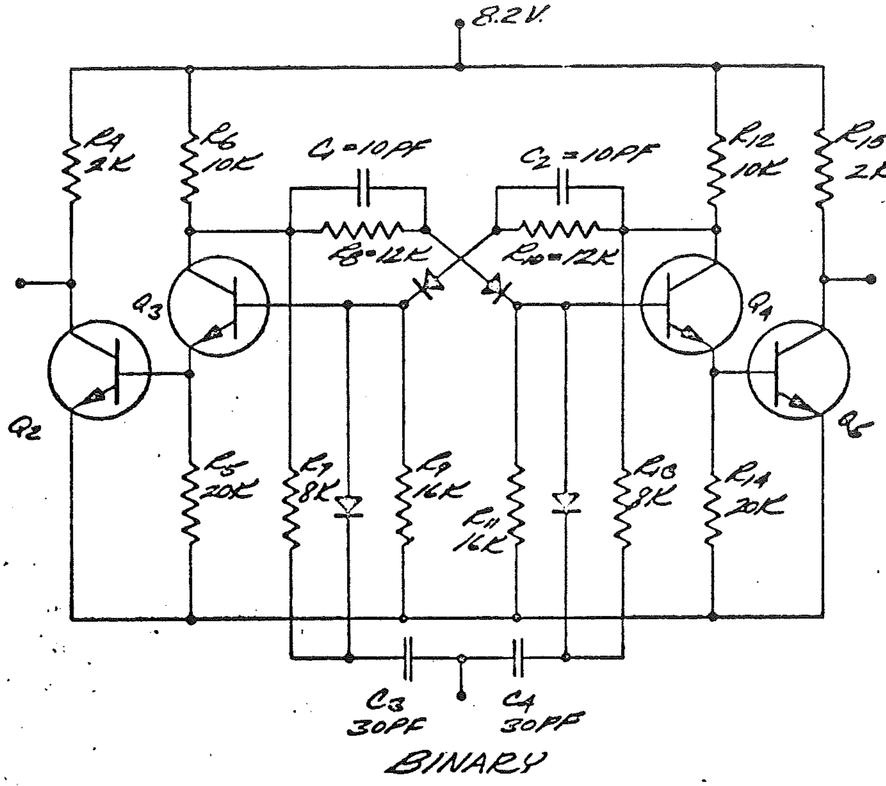


Fig. 22b

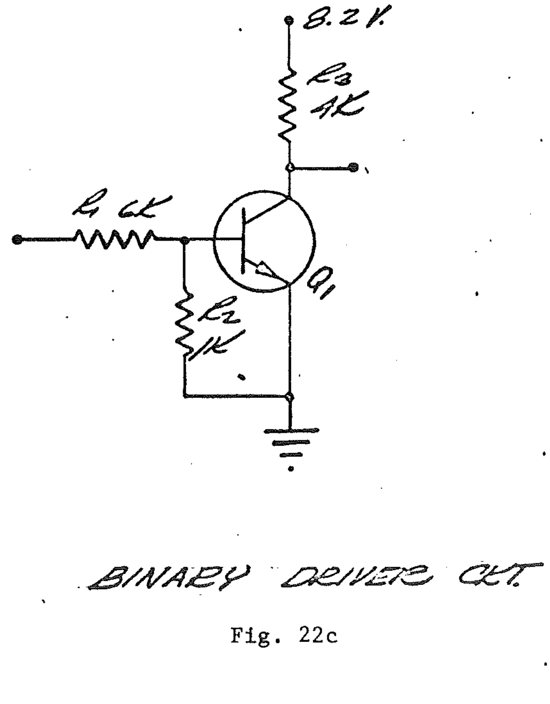


Fig. 22c

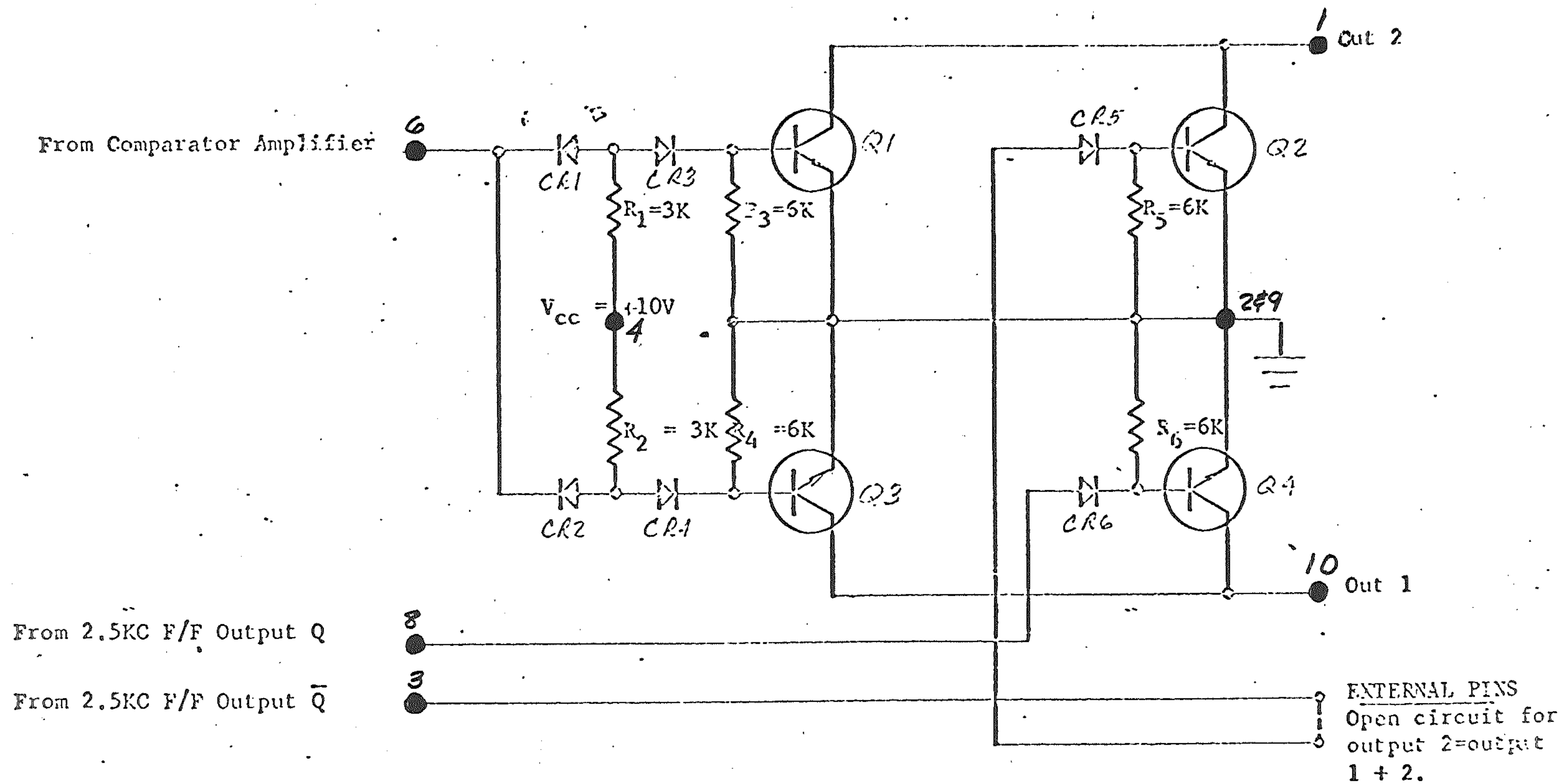


Fig. 22d OUTPUT GATE

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Curve 579815-A

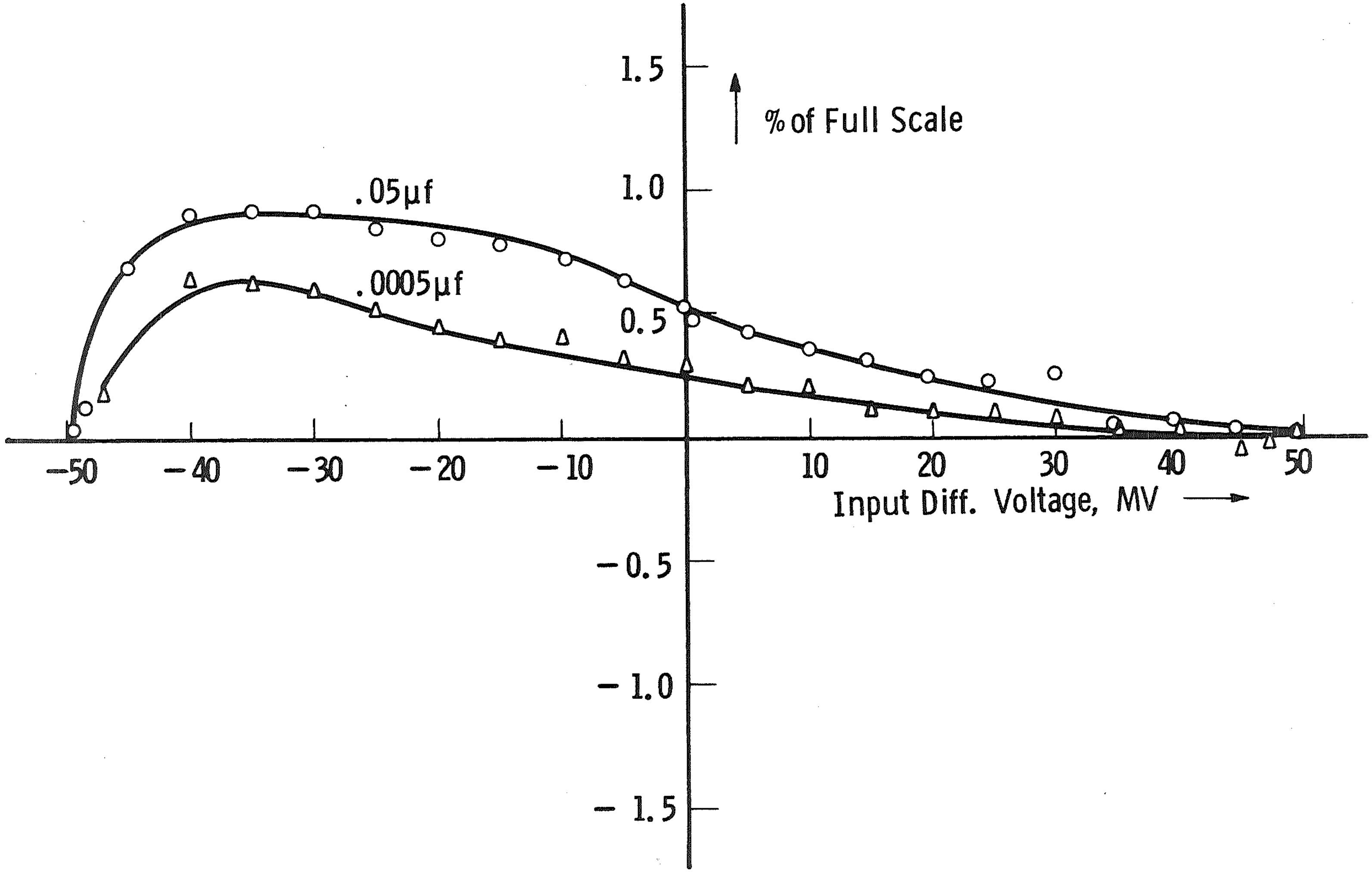


Fig. 23 Analog voltage to duty cycle generator system linearity

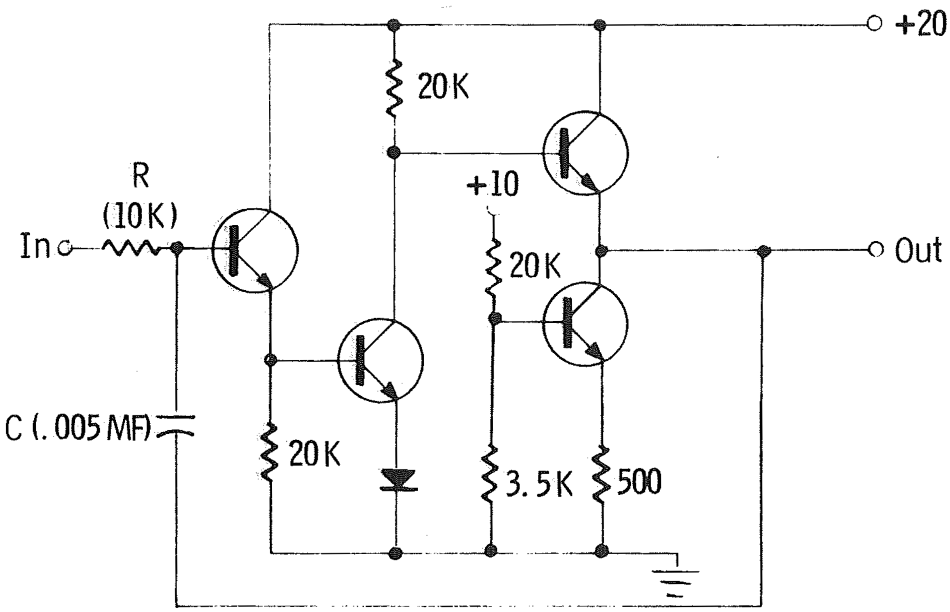


Fig. 24 Single Ended Input Integrating Amplifier

Dwg. 853A637

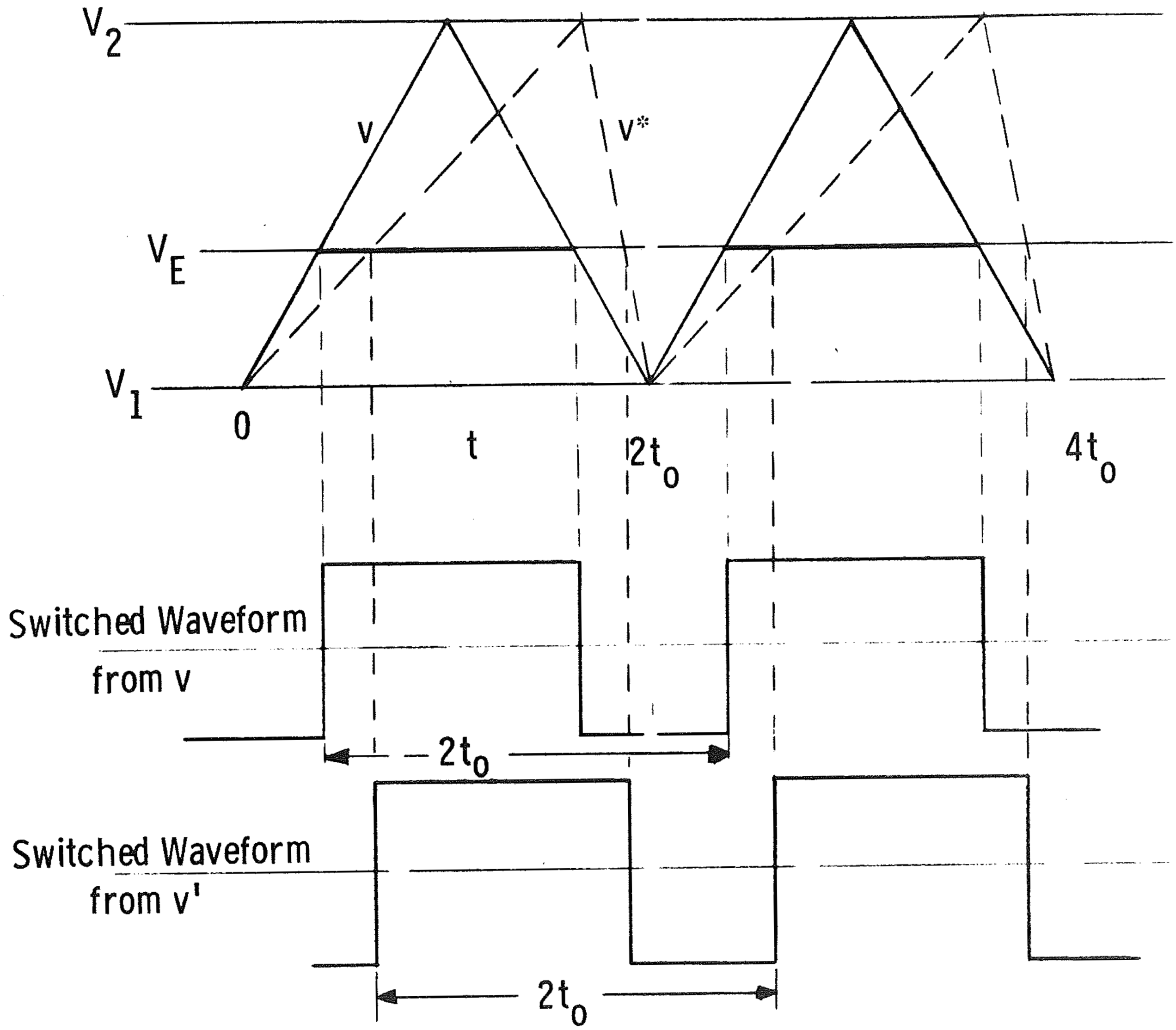


Fig. 25 Effect of Integrating Amplifier Drift on Triangle Waveform

Dwg. 858A241

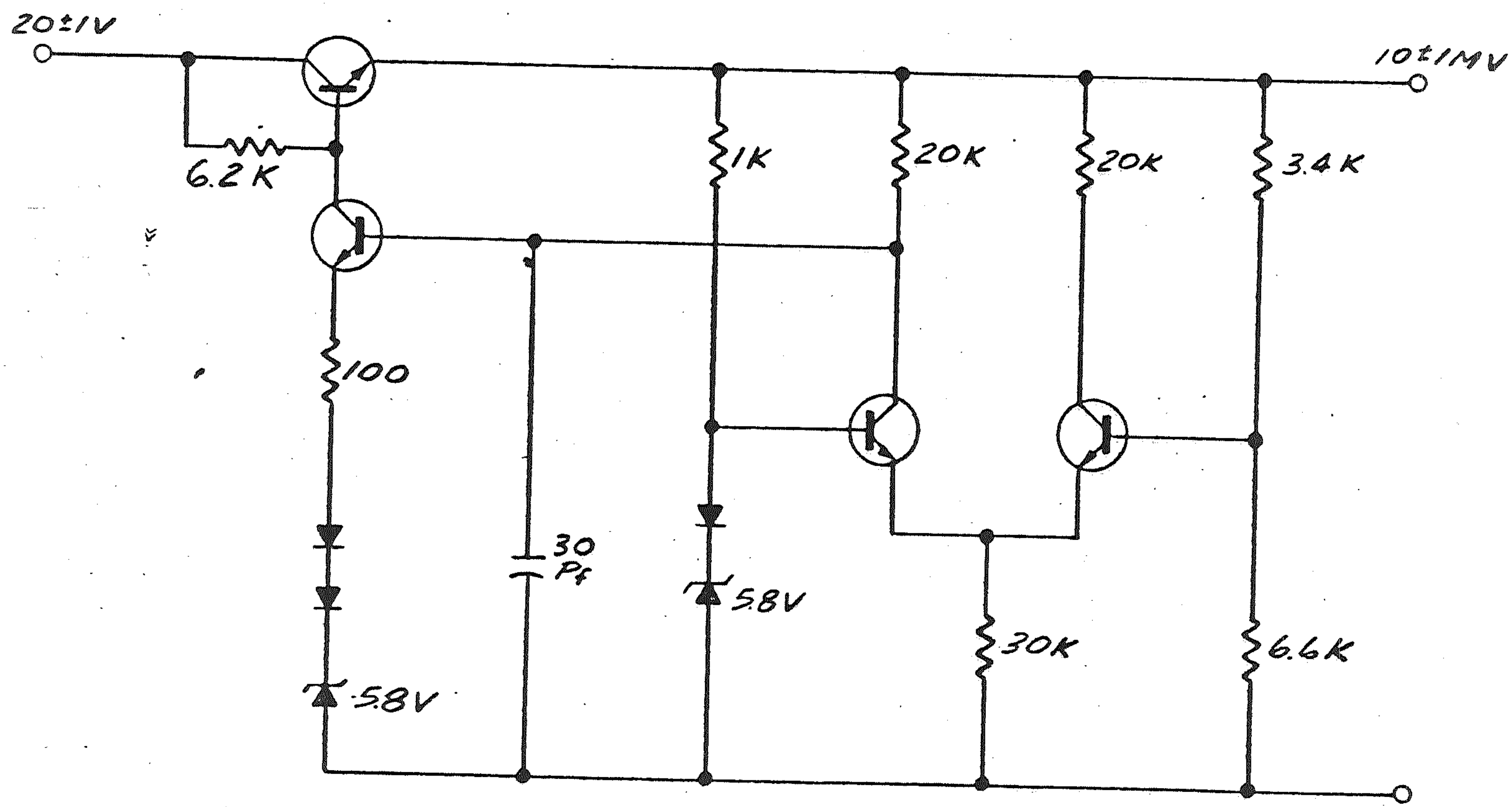


Fig. 26 Voltage Reference Final Design

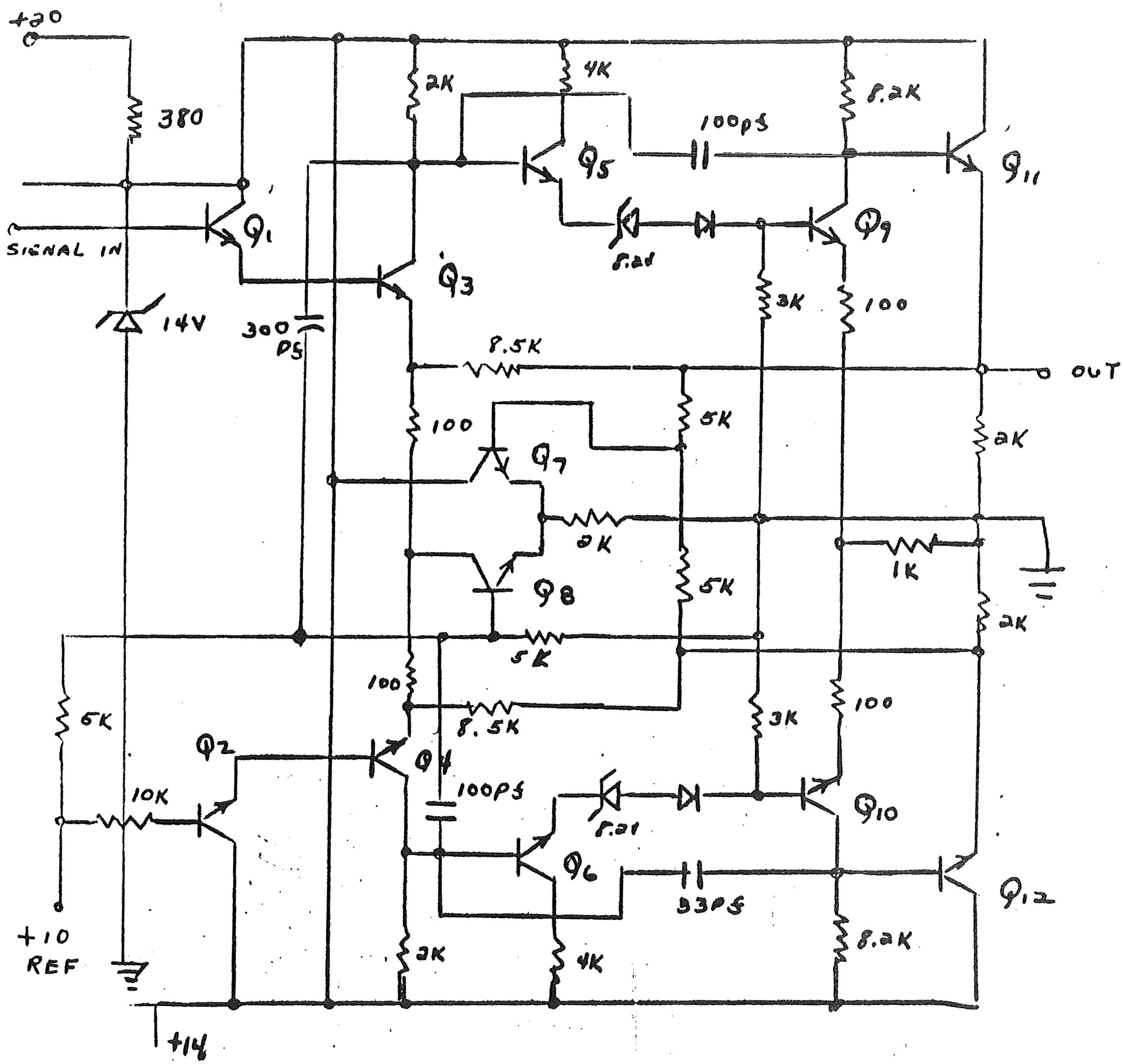


Fig. 27 Error Amplifier Final Design

Dwg. 858A243

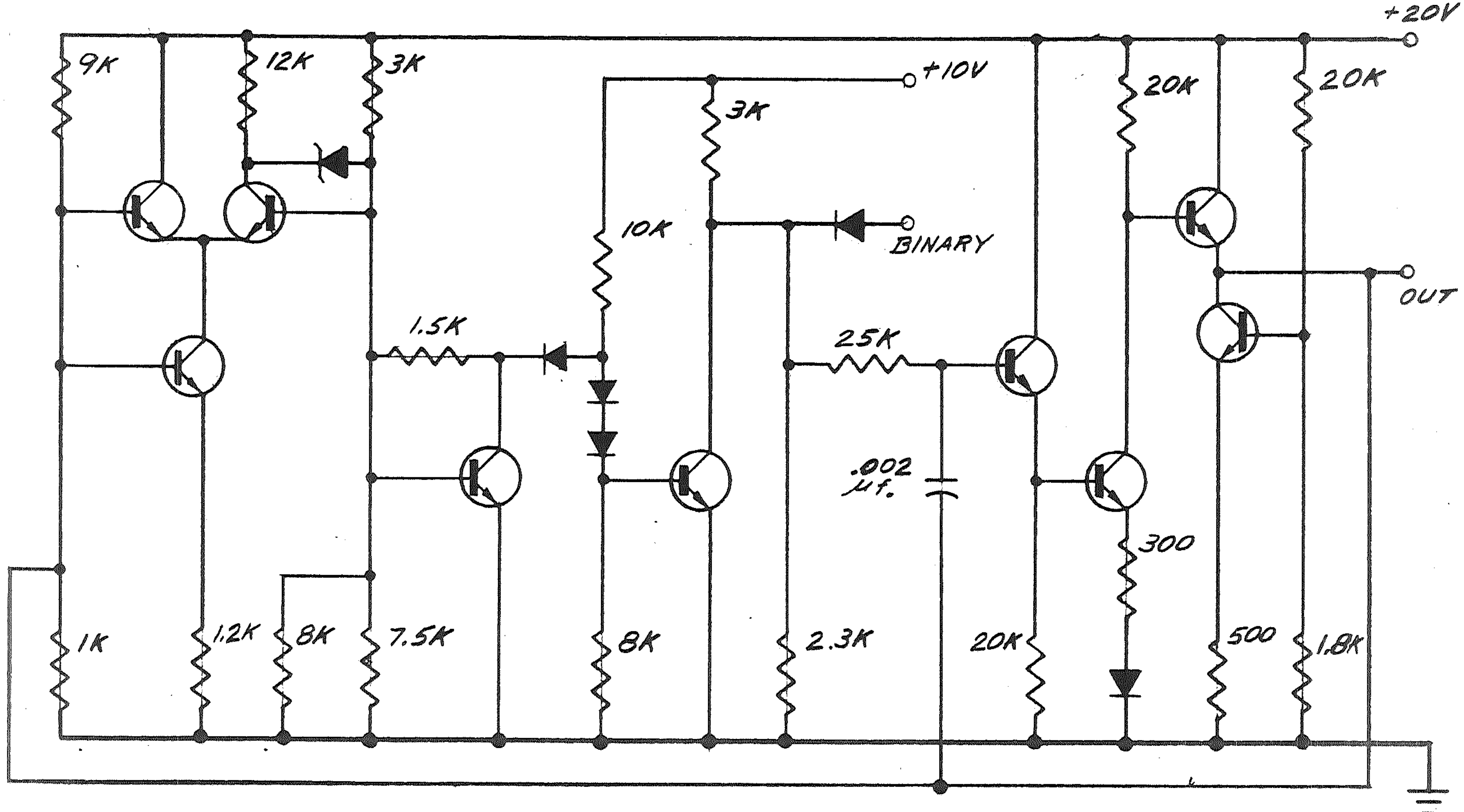


Fig. 28—Triangle generator, final design

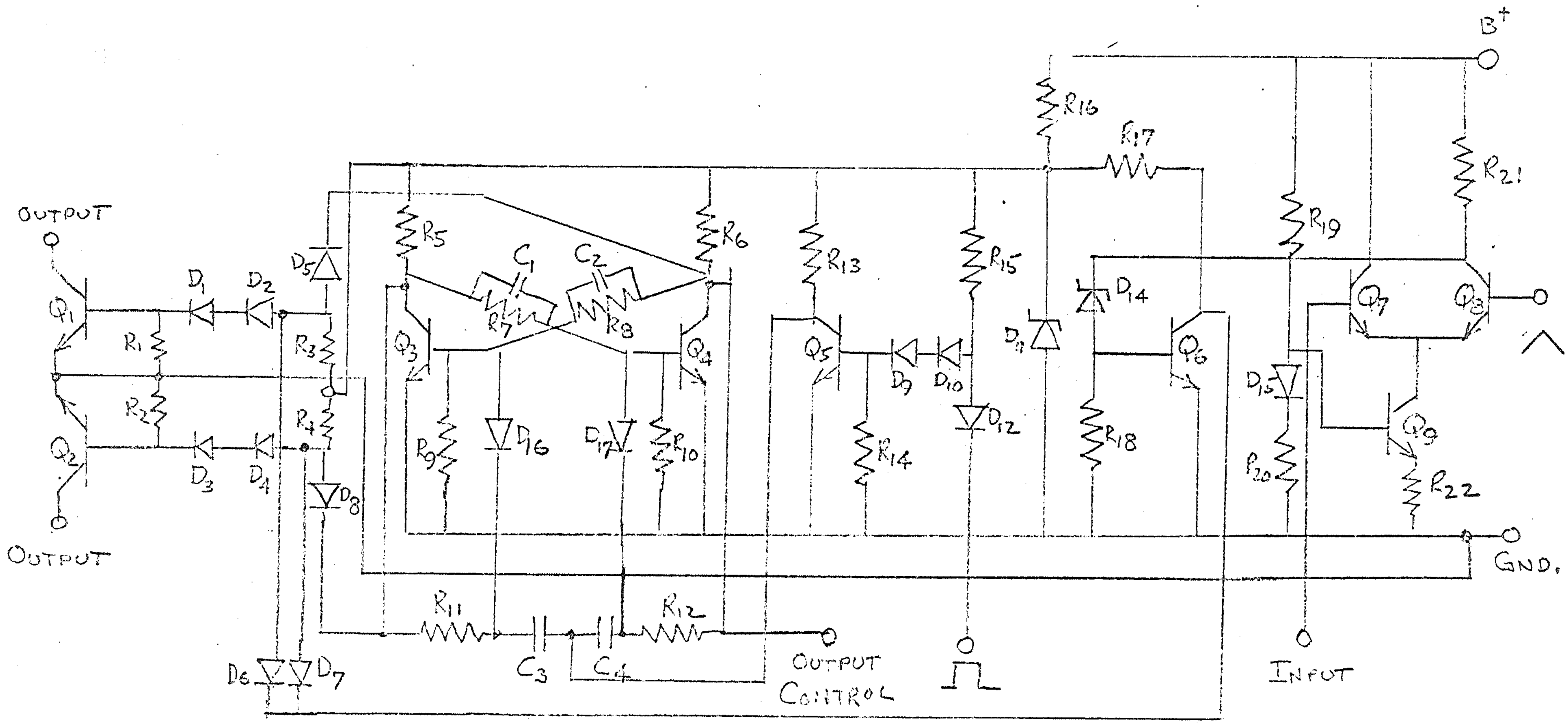
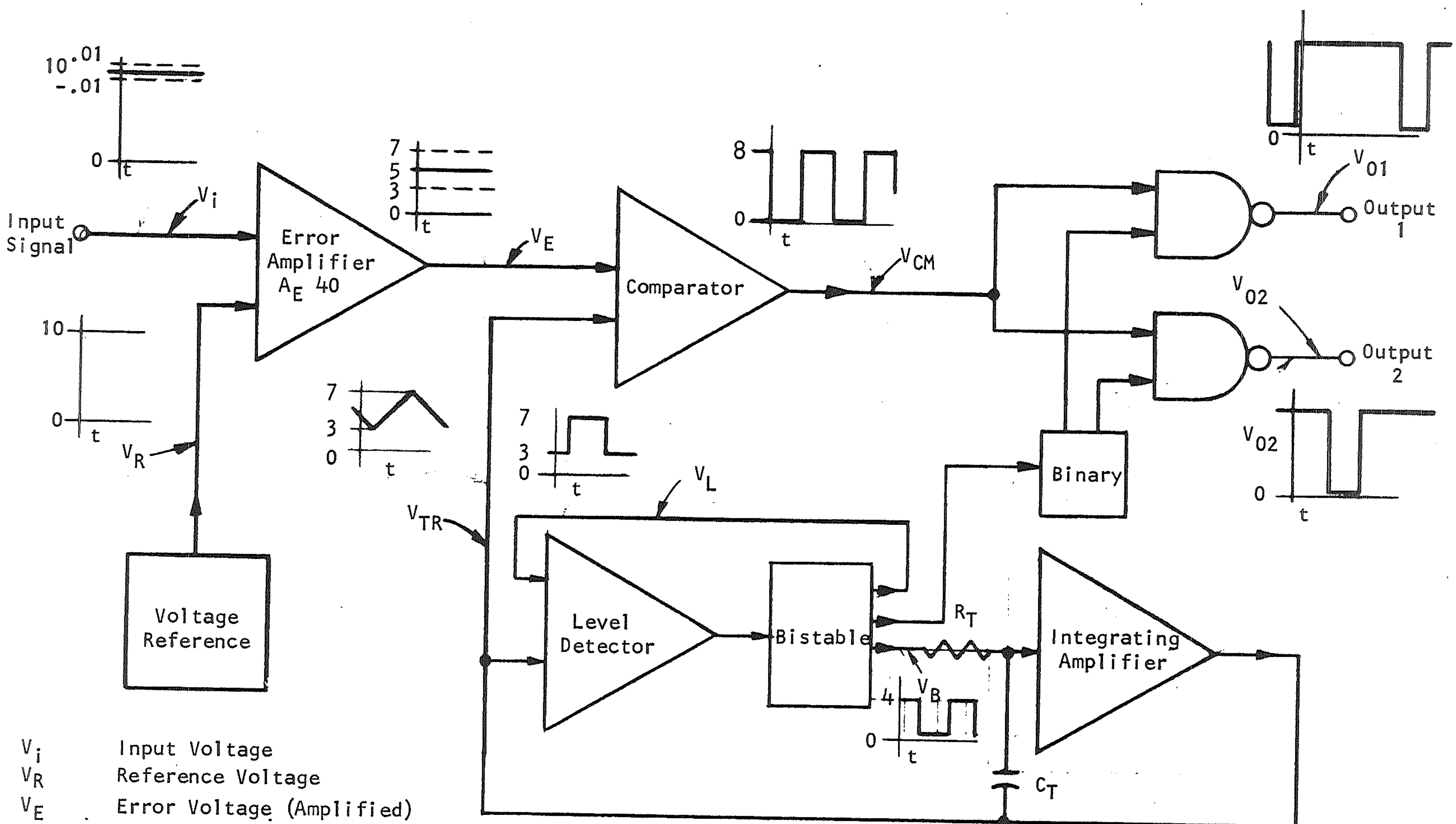


Fig. 29 Ouput Logic Circuitry

Dwg. 858A244



V_i	Input Voltage
V_R	Reference Voltage
V_E	Error Voltage (Amplified)
V_{TR}	Triangular Waveform Voltage
V_L	Level Voltage (Bistable output to level detector)
V_B	Bistable Voltage (Bistable output to integrator)
V_{CM}	Comparator Output Voltage
$V_{01(2)}$	Output Voltage 1(2)
A_E	Error Amplifier Voltage Gain

Fig. 30—Subsystem block diagram, final design, with nominal voltage levels

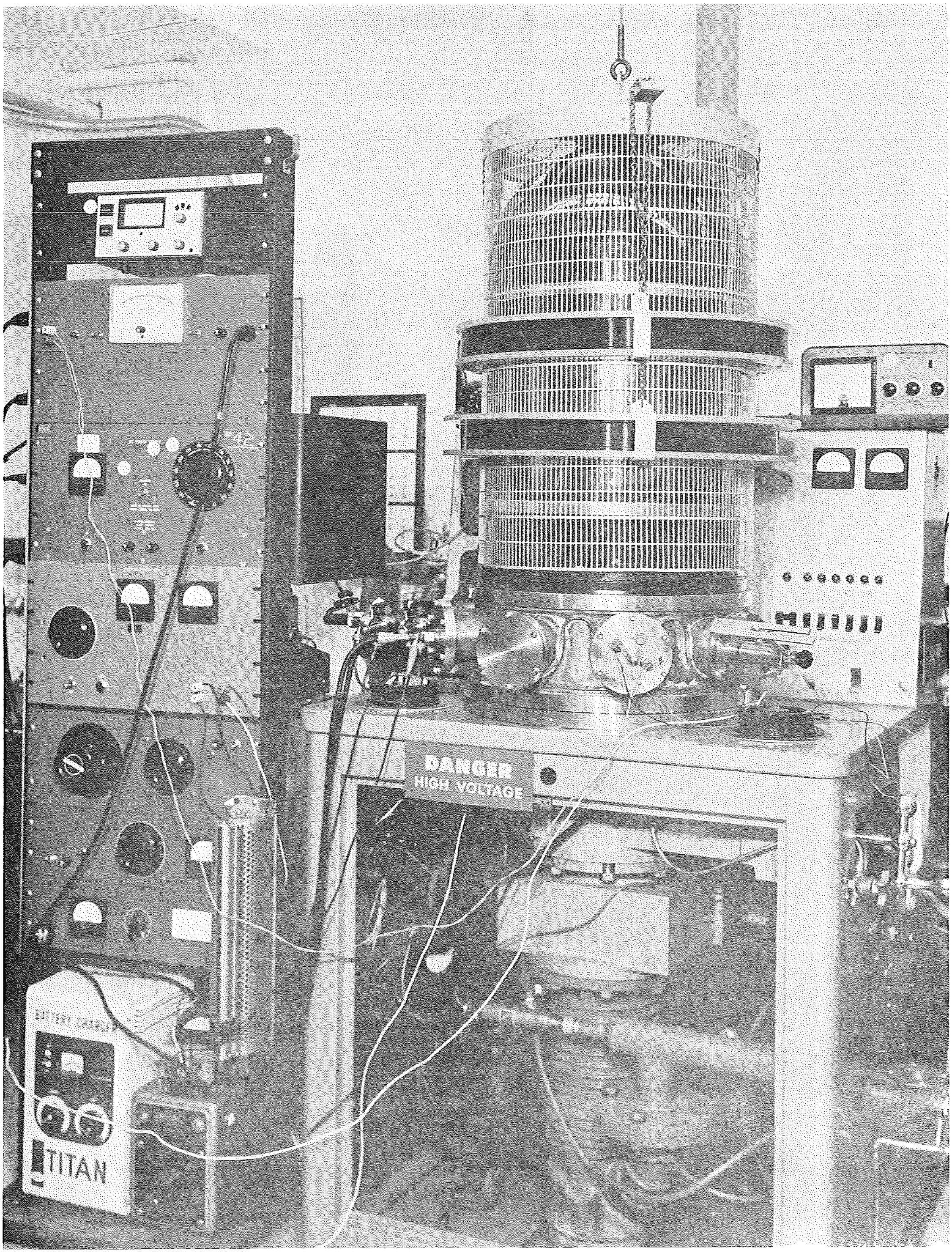


Fig. 31 SPUTTERING SYSTEM

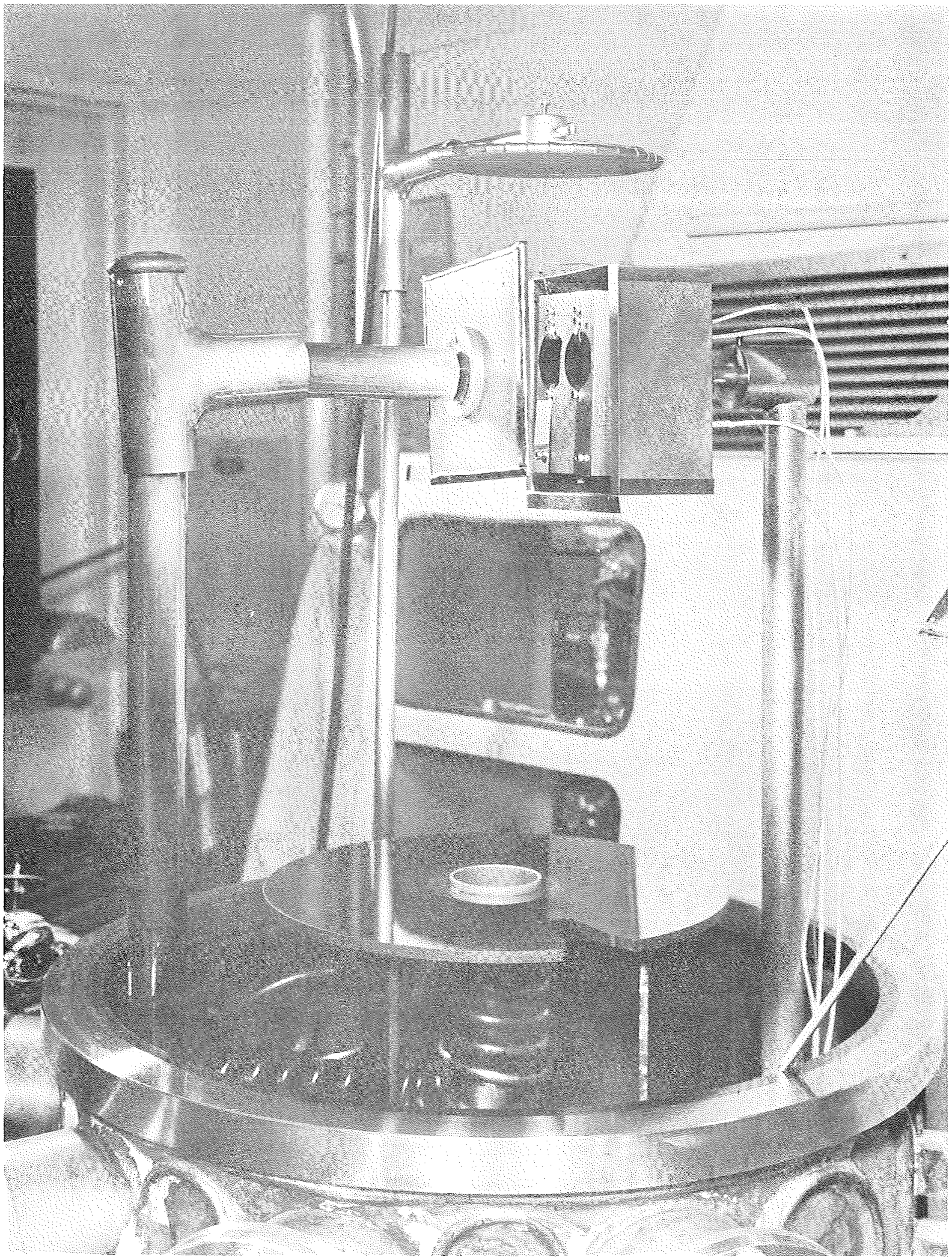


Fig. 32 SUBSTRATE-TARGET-ANODE ARRANGEMENT

Dwg. 855A408

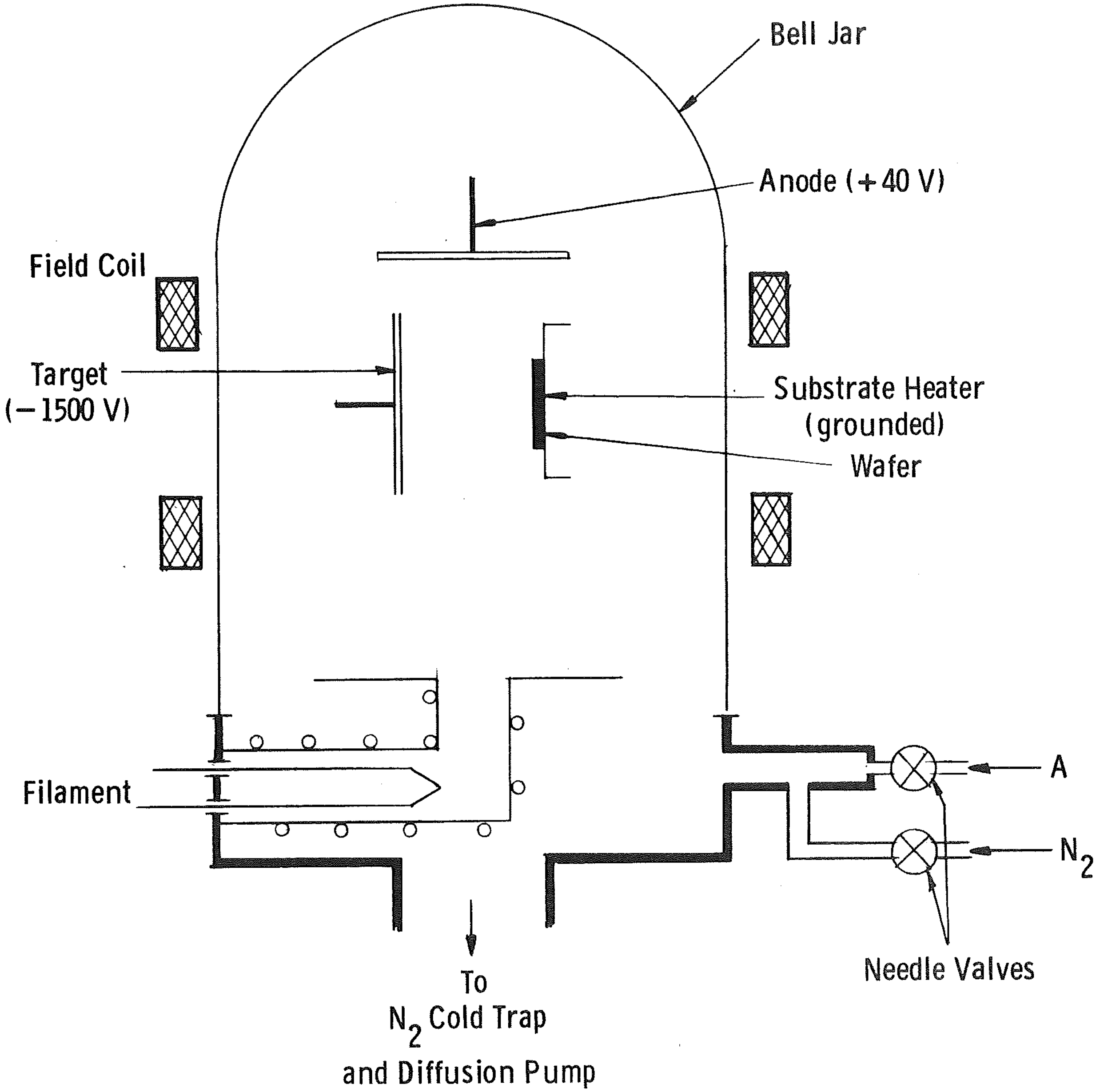


Fig. 33—Schematic outline of triode sputtering system

Dwg. 855A409

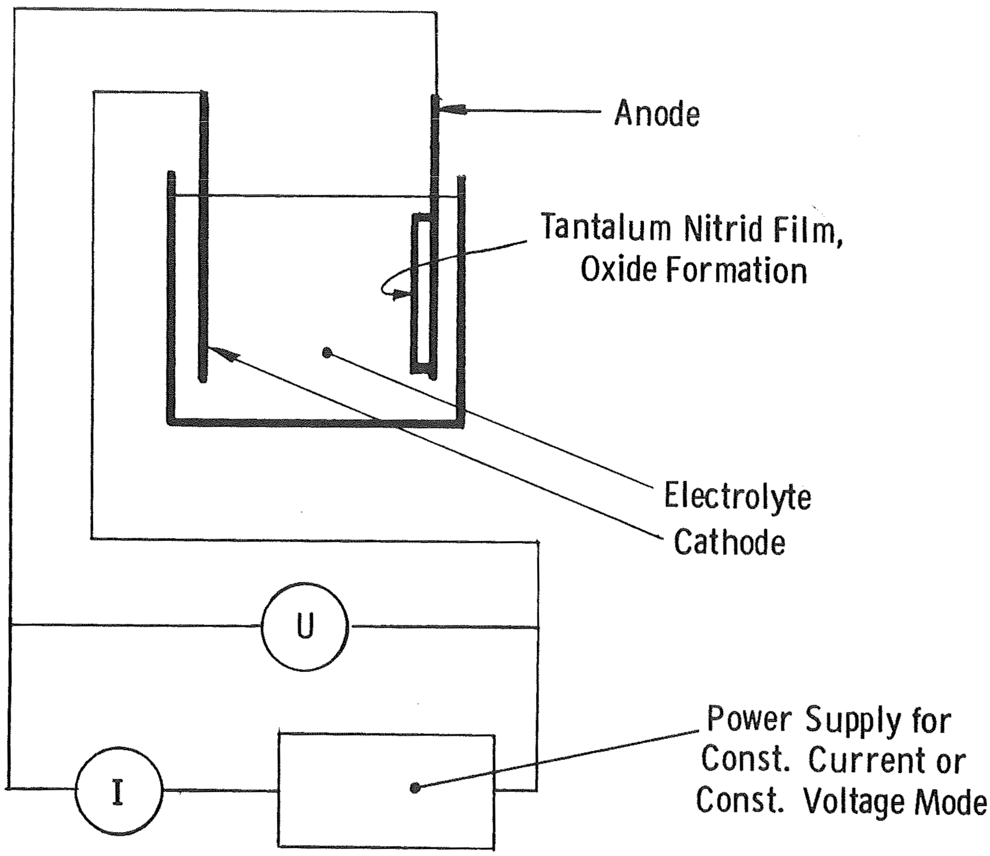


Fig. 34—Anodization

Dwg. 855A410

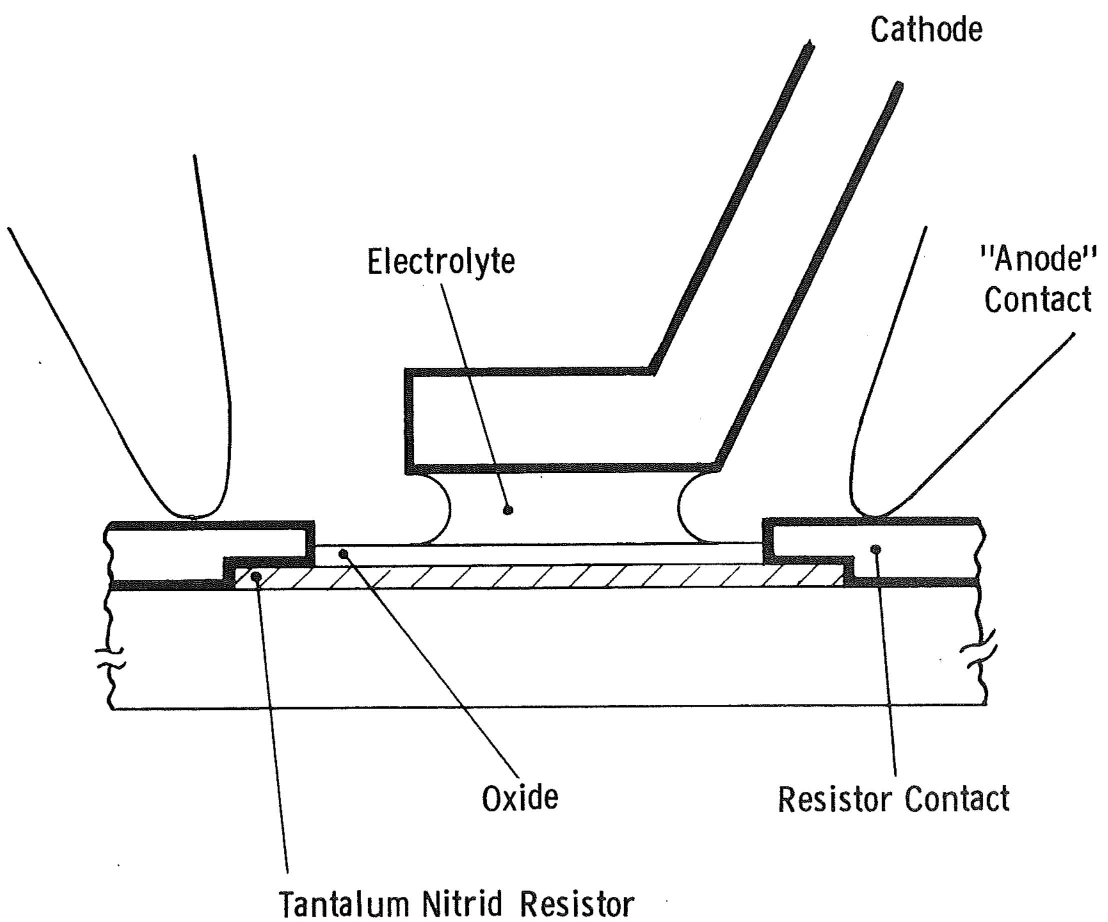


Fig. 35—Trimming with drop anodization

Dwg. 858A245

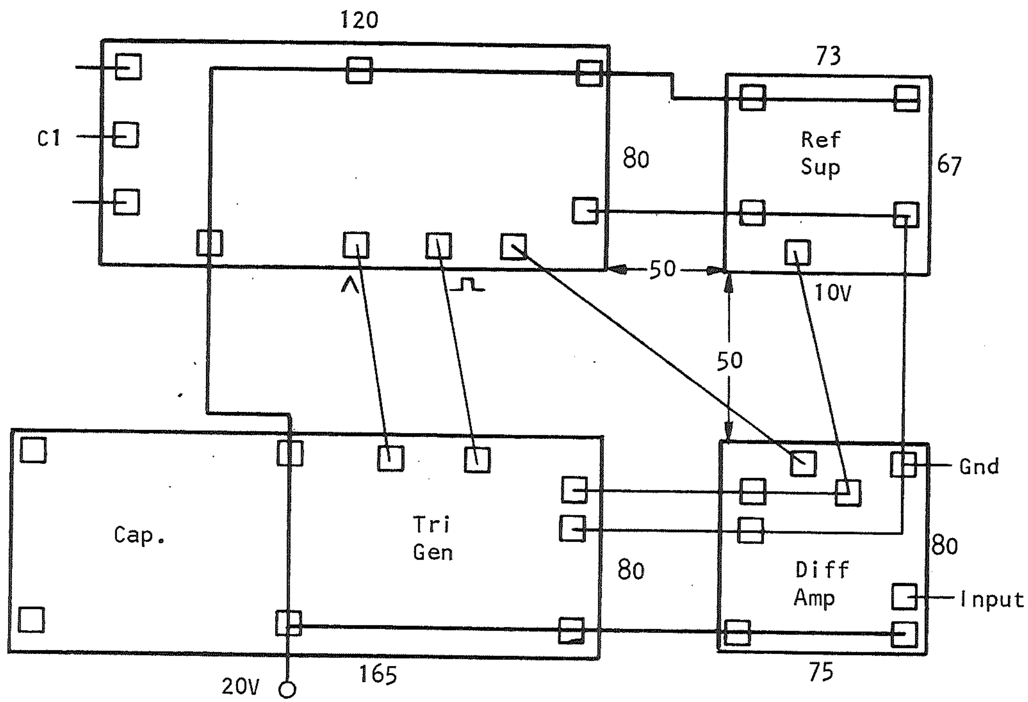


Fig. 36—AVDC system layout

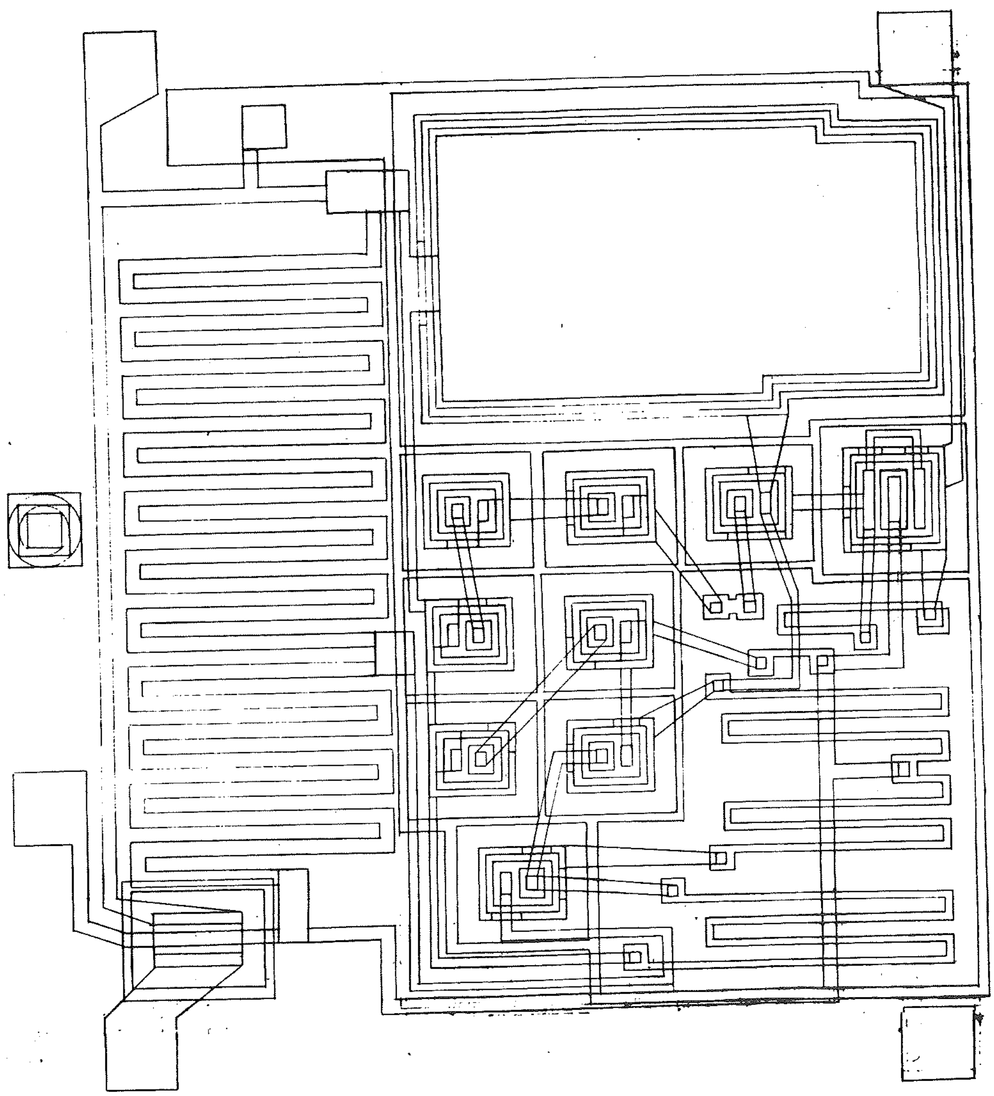


Fig. 37 Reference Supply Layout

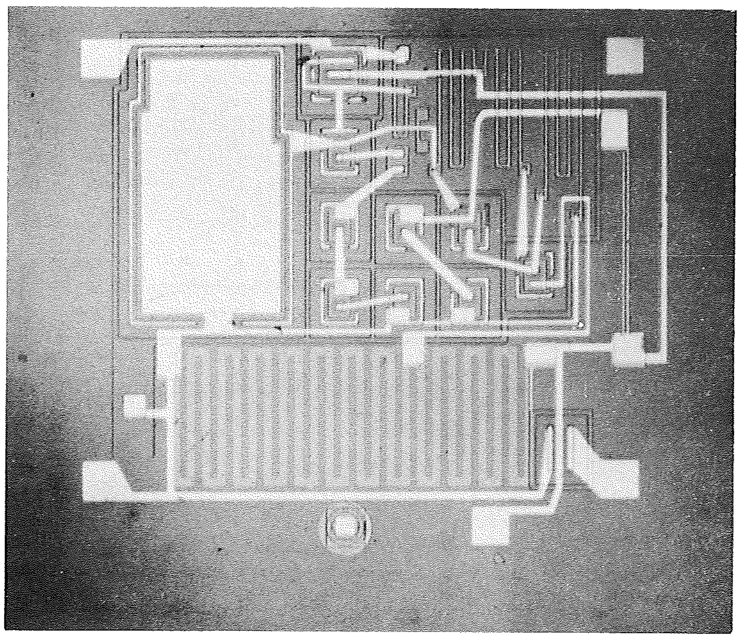


Fig. 38 -- Reference Generator

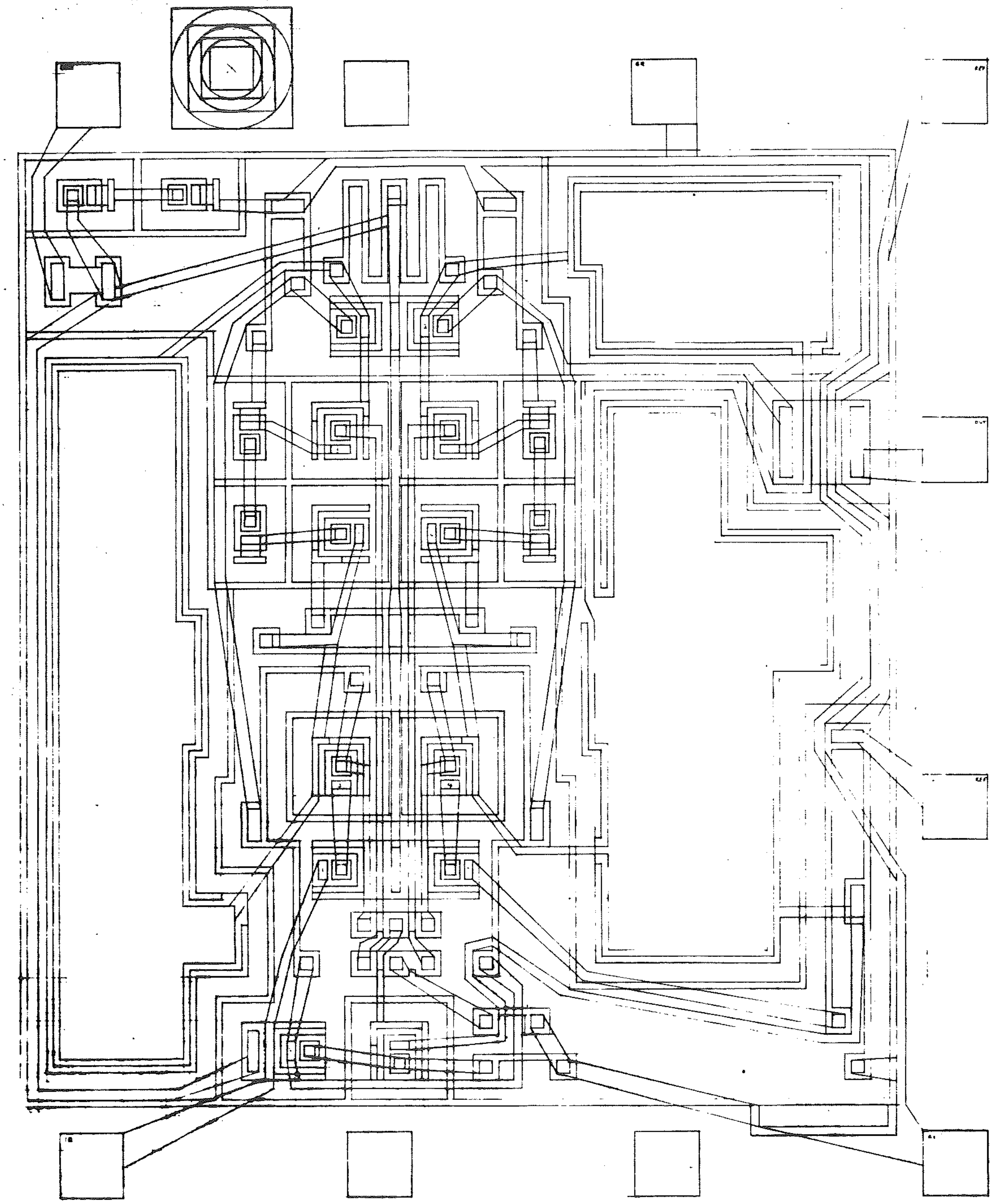


Fig. 39

DR-MOS
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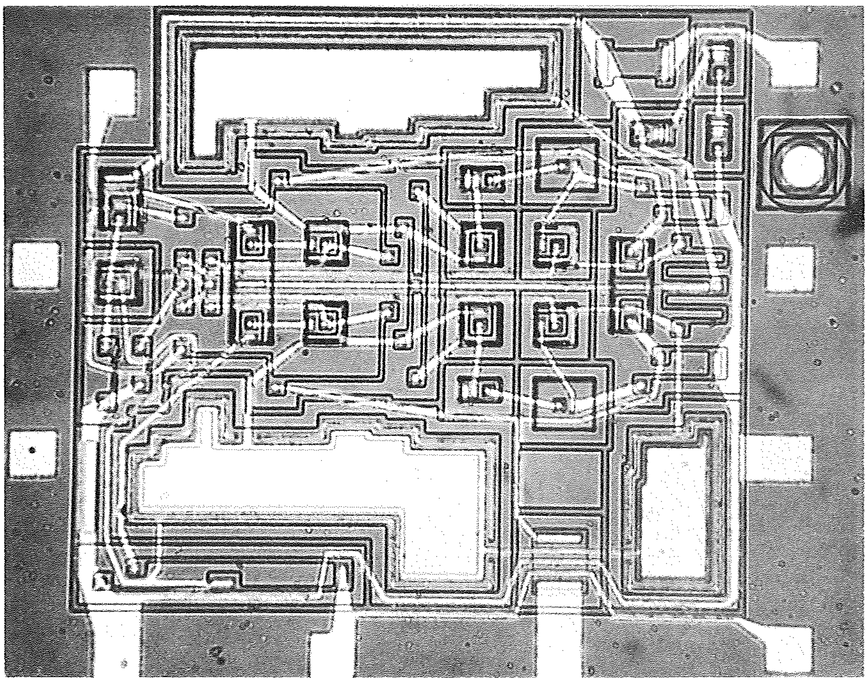

Fig. 40   Differential Amplifier

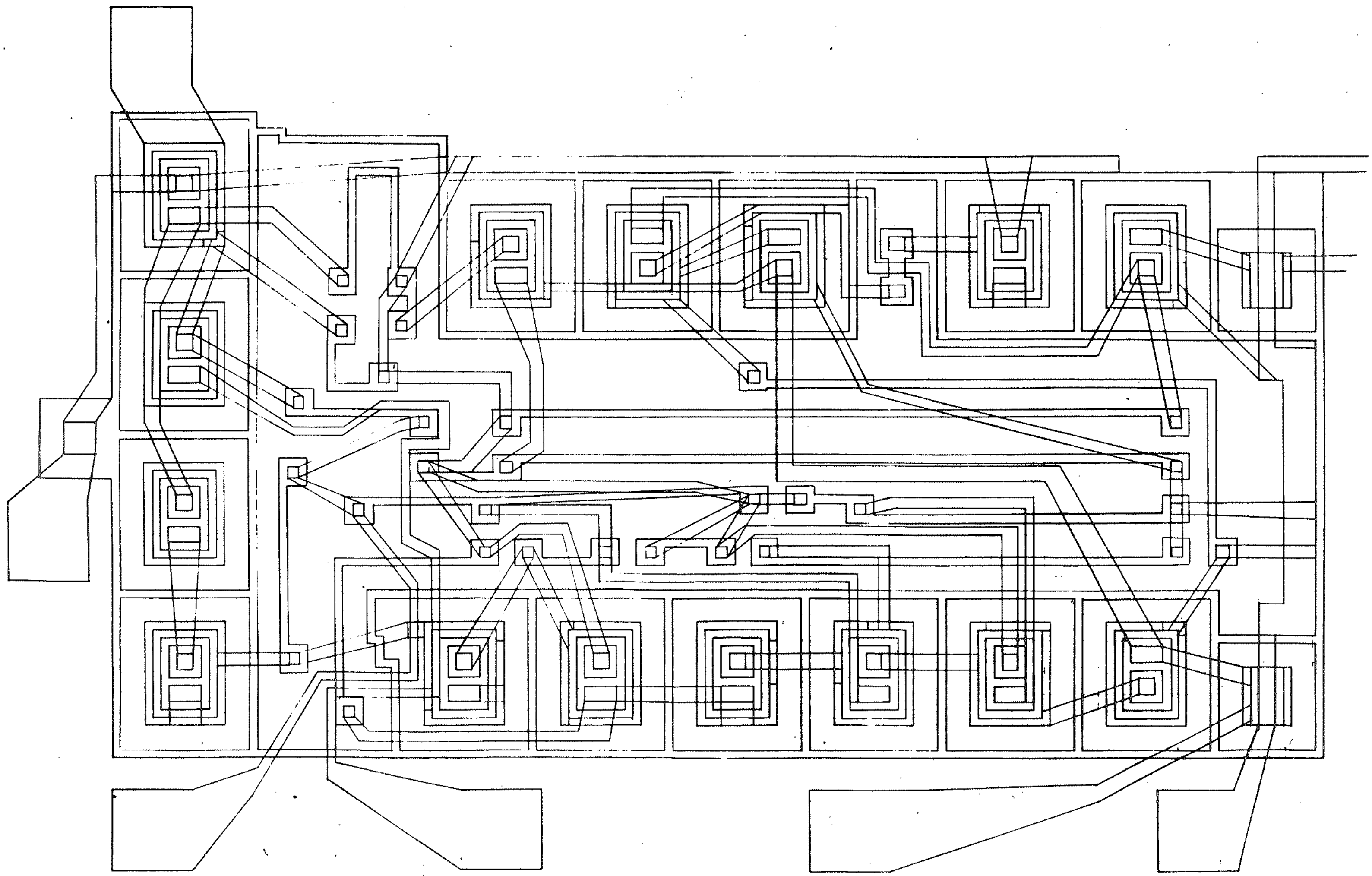

Fig. 41 **Triangle Generator Layout**

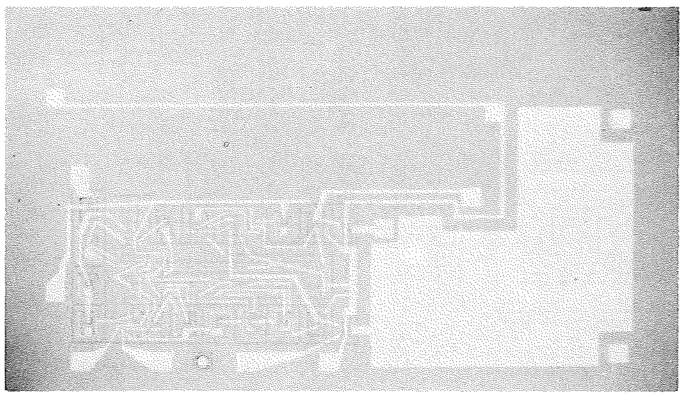

Fig. 42 Triangle Generator

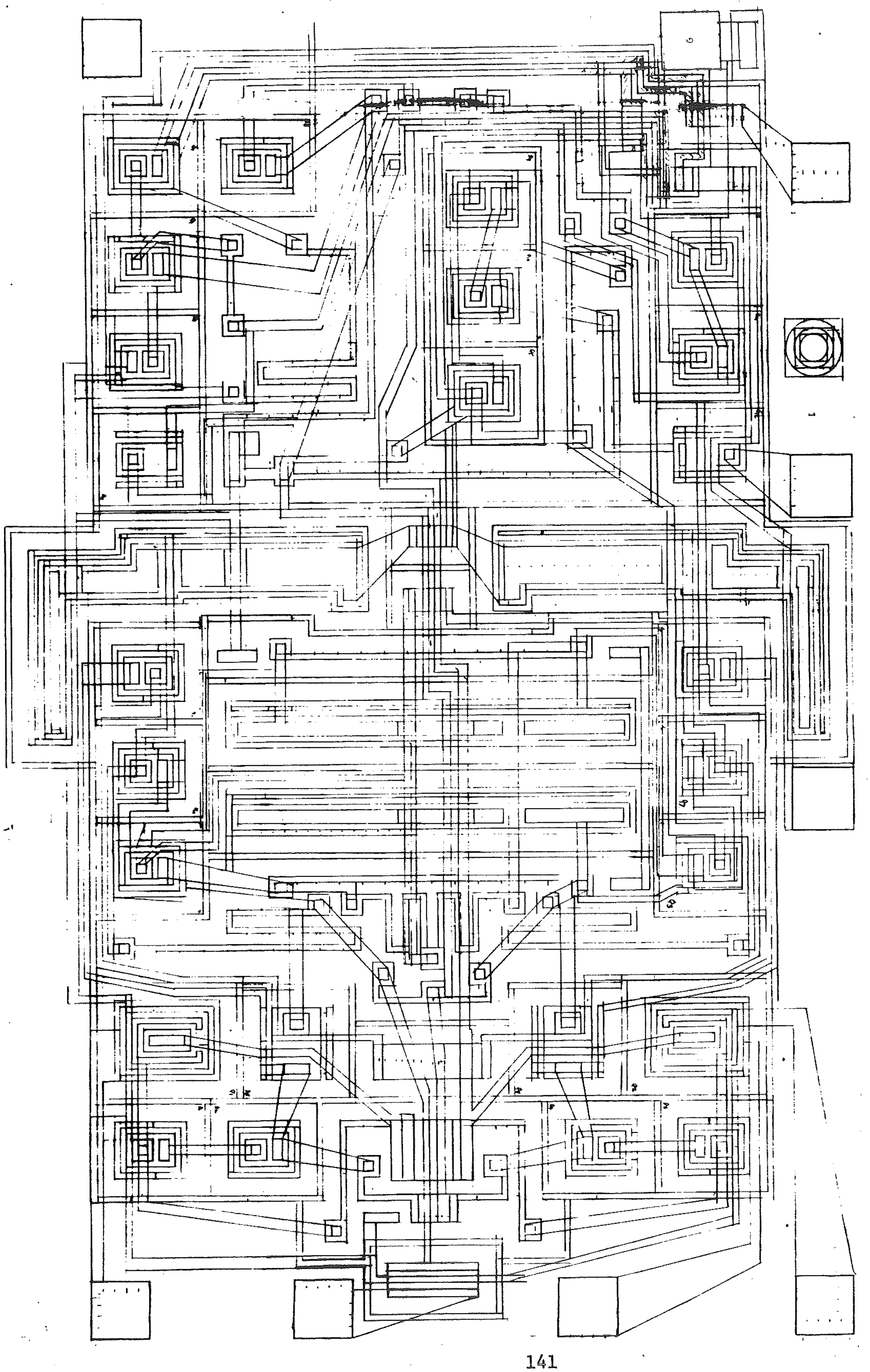

Fig. 43 Output Circuit Layout

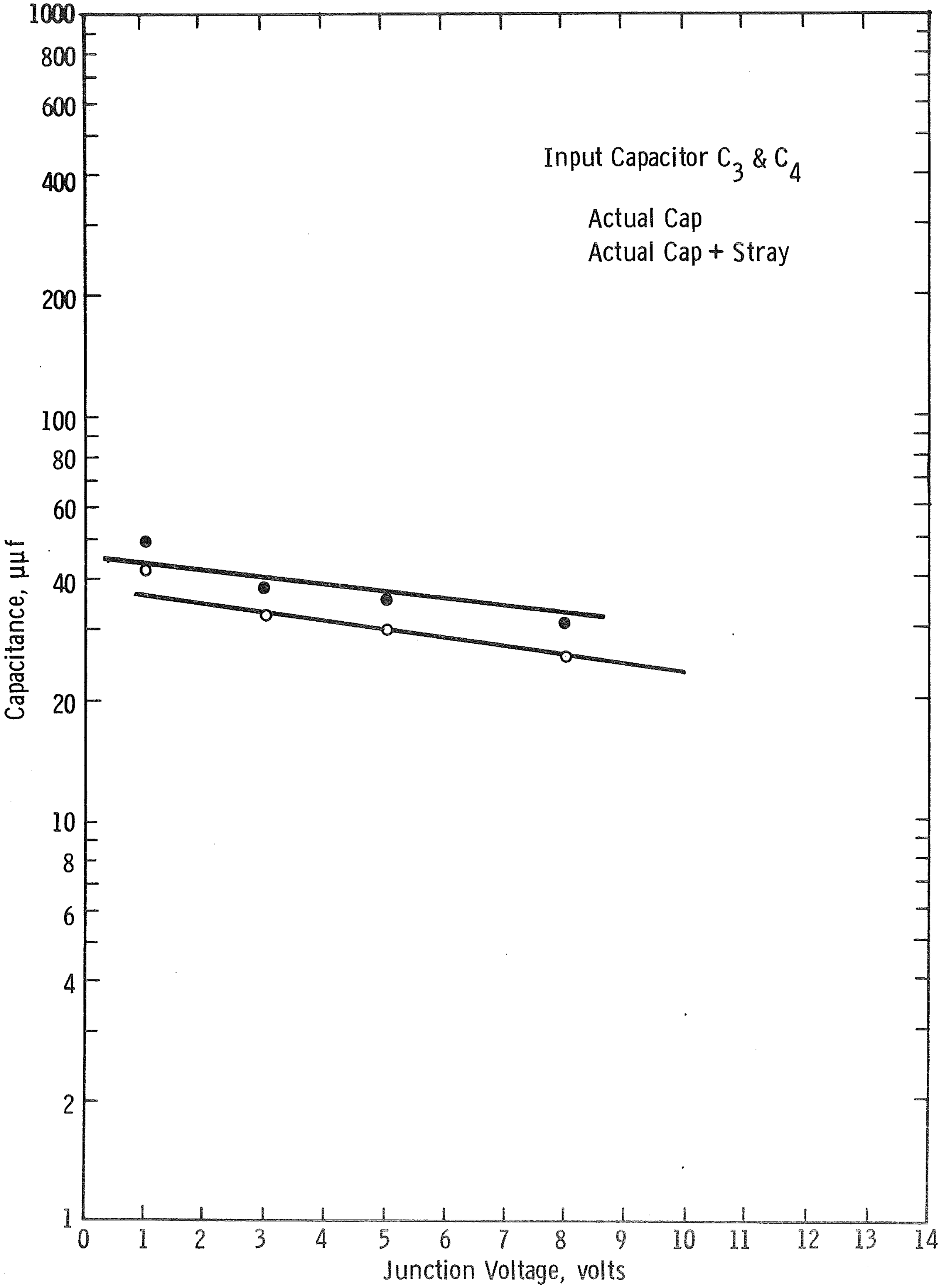

Fig. 44—Junction capacitance vs voltage for JPL output logic

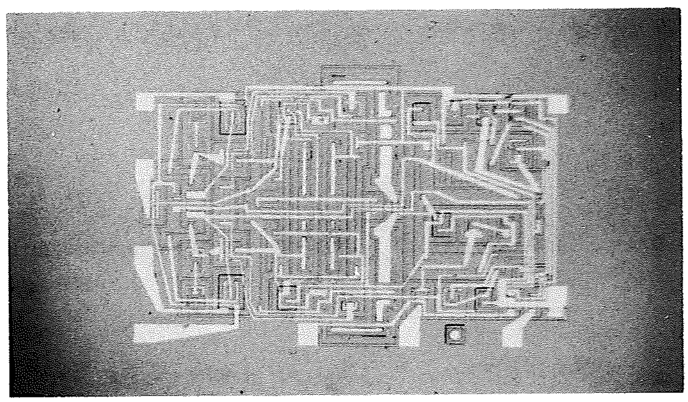

Fig. 45   Output Circuit

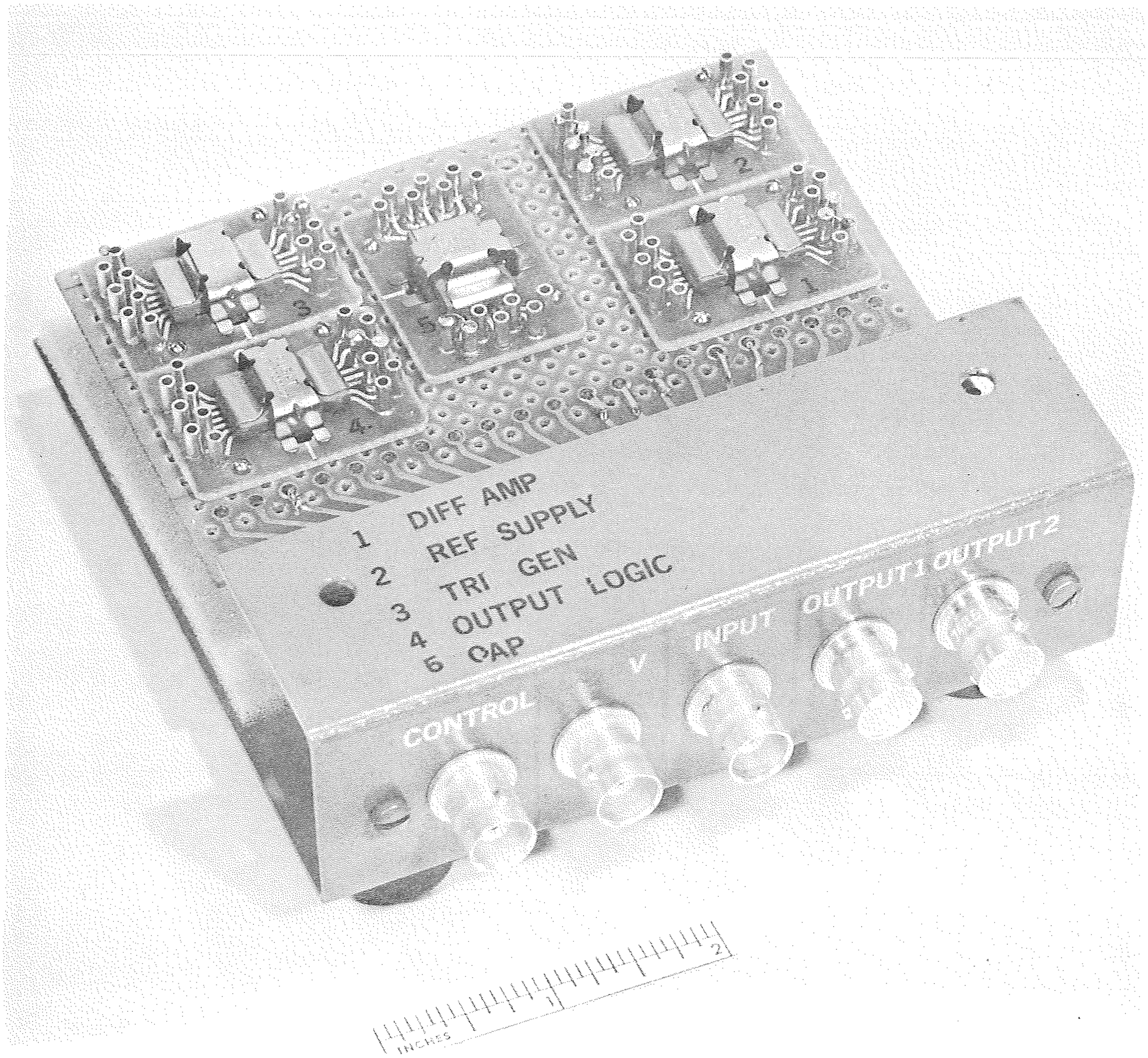

Fig. 46 - Test Fixture

DWG. 858A425

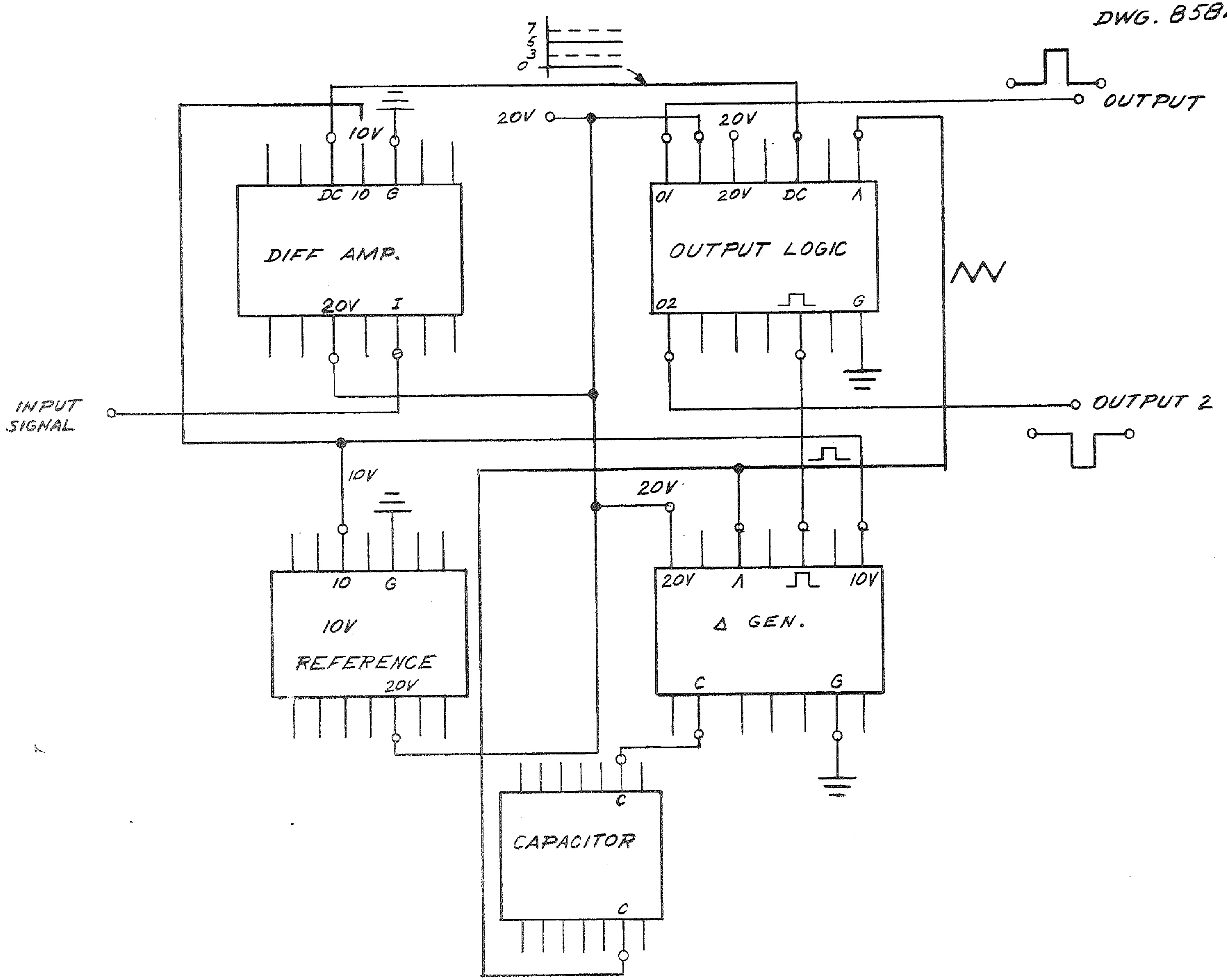

FIG. 47 FLOW DIAGRAM OF PACICAGED CIRCUITS